Kufa Journal of Engineering
Vol. 15, No. 2, April 2024, P.P. 16-26
Article history: Received 25 July 2023, last revised 22 December 2023, accepted 26 December 2023

HIGHLY EFFICIENT INVERTER BLOCKS IN QCA TECHNOLOGY

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https://doi.org/10.30572/2018/kje/150202

ABSTRACT

QCA technology presented as a new paradigm to replace CMOS technology in the nanoscale. QCA technology represents binary information by cell polarization, not as a voltage level. The basic blocks in QCA technology are the majority gate and inverter. Efficient building blocks are important to get whole efficient circuits. This article aims to present novel configurations for the inverter block that offer advantages in terms of temperature tolerance, cell count, and area efficiency. Moreover, a Repeater gate with high efficiency is proposed to demonstrate their versatility. The proposed inverter has efficient improvements by 2%, 4.4%, 11%, and 17.5% over the best-reported inverter block at 10 K, 100 K, 150 K, and 200 K, respectively. The circuits presented in this study were designed and validated using QCADesigner software v 2.0.3, and the energy consumption of the proposed designs was assessed using QCAPro tools.

KEYWORDS: QCADesigner, Inverter block, Nanoelectronic circuit, QCA Technology.

1. INTRODUCTION

As a result of the physical constraints of CMOS technology, such as power dissipation in the nanoscale and short channel effects, researchers have explored alternative technologies to enable continued scaling of transistors in a chip as predicted by Moore's law. Carbon Nanotube-Field Effect Transistor (CNTFET), Single Electron Transistor (SET), and Quantum-dot Cellular Automata (QCA) are among the nanotechnologies that have been proposed as competitors. In 1993, Lent et al. introduced QCA technology as a new paradigm for binary representation (Lent et al, 1993). QCA uses the quantum properties of electrons to store data and for calculations, giving it advantages such as deficient power consumption, ultra-fast operation, and remarkable miniaturization. Despite its potential, it suffers from challenges such as environmental sensitivity and manufacturing complexity, which necessitates continuous research for practical implementation. The diversity of QCA extends to logic circuits, memory devices, and communications systems. As researchers address the challenges and improve the technology, QCA is a promising technology to revolutionize the nanotechnology landscape and redefine the possibilities of computation. Some of these challenges are circuit temperature tolerance, area occupancy and cell count. This paper will introduce novel configurations of the inverter block, one of which is used to design a four-level repeater circuit.

This work will be organized as follows. Section 2 will focus on the basics of QCA, Section 3 on previous work, Section 4 on the proposed design, Section 5 will present the output waveforms as a simulation and comparison result, and Section 6 will be devoted to conclusions.

2. QCA FUNDAMENTALS

QCA technology utilizes the principle of electron repulsion, where each cell is square-shaped and contains two free electrons that can tunnel between four holes (dots) inside the cell. Each cell must be in one of two possible states, depending on the driving cell, with the cell having polarization equal to -1 representing logic 0, and the cell with polarization +1 representing logic 1. This is illustrated in Fig.1 (Majeed et al., 2020b, Majeed et al., 2019a).

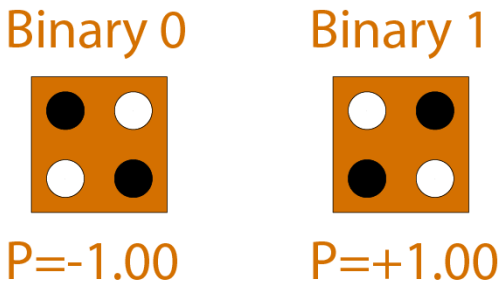

Fig. 1. QCA cell configurations.

QCA technology relies on two fundamental building blocks: the inverter and the majority voter. Fig.2 shows the majority voter, which is constructed from five cells and can form AND and OR operations by fixing one of the five inputs to polarization -1 and +1, respectively. The majority block in high order, meaning more than three inputs, has also been studied in previous work (Kassa and Nagaria, 2016, Majeed et al., 2020a, Sasamal et al., 2016, Majeed et al., 2019b). A chain of cells represents a binary wire where each cell must adopt the same polarization as the preceding cell, based on the principle of electron repulsion, as demonstrated in Fig. 3. The clock signal is essential in QCA technology for controlling signal direction and addressing synchronization issues. The clock signal governs the barriers between holes and operates in four phases: Relax, Switch, Hold, and Release. These four states operate sequentially to maintain circuit stability. To ensure signal refreshing and power stability, the QCA circuit can be divided into four separate zones, each marked with different cell colors and operating in a distinct clock cycle, as shown in Fig.4.

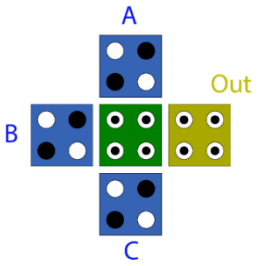

Fig. 3. Cell configurations of majority block.

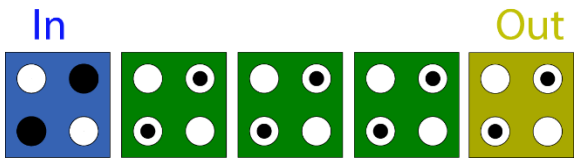

Fig. 2. Cell configurations of (a) binary wire.

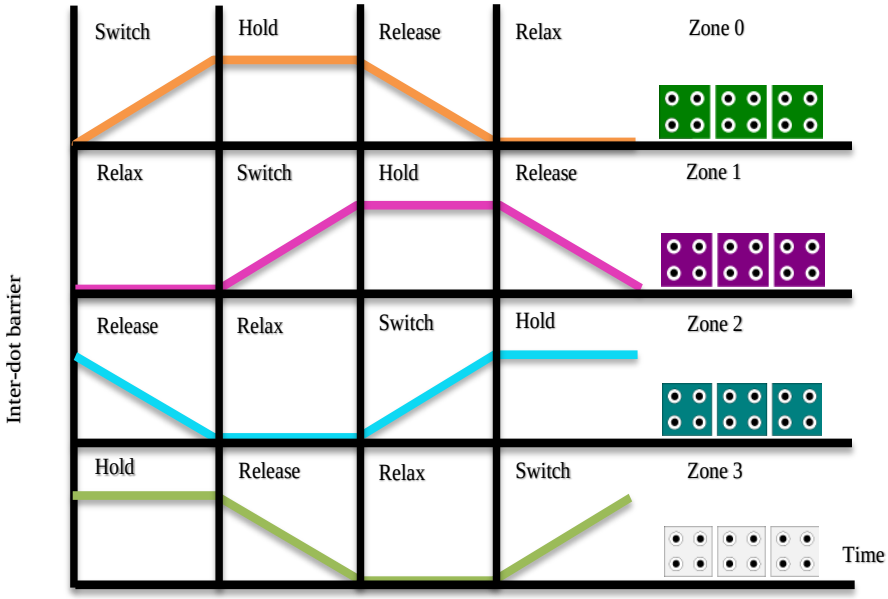

Fig. 4. Clock signal zones and phases.

3. RELATED WORK

In QCA circuits, the efficacy of building blocks in terms of polarization level and temperature tolerance are critical challenges because of the signal transfer from cell to cell as a polarization-states. In the literature, many structures of QCA-inverter were presented. Some of them use rotated cells by 90º (Goswami et al., 2020, Zahmatkesh et al., 2019, Tougaw and Lent, 1994, Khan and Chakrabarty, 2013). Regular-cell blocks are preferred in QCA technology, as introduced in (Tougaw and Lent, 1994, Beard, 2006, Kalogeiton et al., 2017, Kumar and Mitra, 2016). Fig.5 presents the different structures of the QCA inverter, as shown in the figure explanation. Fig.5 (a) shows the rotated cell inverter. This innovative approach introduces round cells in the structure, which may provide distinct advantages in terms of function and performance. Fig. 5 (b) represents the most commonly used QCA inverter design, which serves as a standard configuration in many QCA-based systems. It is a widely used structure. Fig. 5 (c) presents the design of the QCA inverter incorporating highly polarized cells. By incorporating highly polarized cells, this structure aims to enhance the polarization effect, leading to improved signal propagation and reliability within the QCA system.

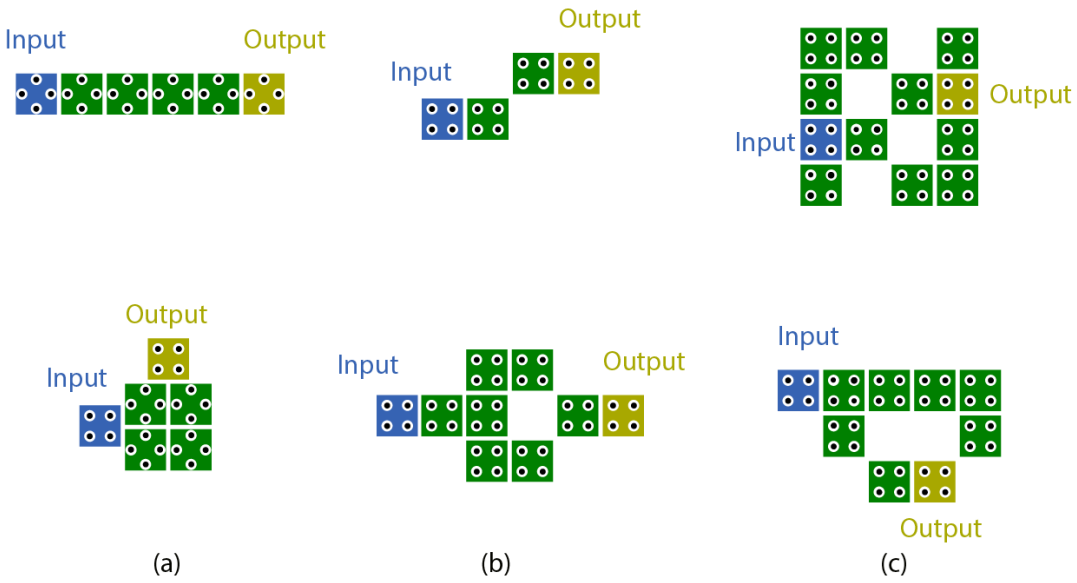

Fig. 5. Different structures of QCA-inverter (a) using rotated cells (Tougaw and Lent, 1994, Goswami et al., 2020) (b) commonly used (Tougaw and Lent, 1994) and (c) high-polarization (Zahmatkesh et al., 2019, Kumar and Mitra, 2016).

4. PROPOSAL DESIGN

As mentioned before, the circuit with one-type cells is preferred in QCA technology (Angizi et al., 2014). Therefore, this paper proposes three different structures of inverter block that use only normal cell types with high polarization and temperature tolerance. Fig. 6 illustrates the proposed three forms of inverter block. All three styles are high-polarization, but the inverter

with high cells is high level than the others. Inverter cells can be used as a building block in other circuits such as adders (Zhang et al., 2018), RAM (Sasamal et al., 2018), and multiplexers (Mallaia et al., 2018). Nowadays, circuit designers have new challenges because there are several applications, and each application needs specific requirements. So, introducing universal building blocks is vital in providing a new attribute for electronic circuit designers. In addition, when a circuit designer wants to provide a plan to solve embedded design problems, the availability of different kinds of building blocks leads to increased flexibility. Considering the proposed design advantages when an application needs to have a high range fanout and high polarization, the proposed inverters can be helpful to drive logic values. Moreover, there are two solutions in circuits to keep high-polarization signals power on the circuit. First, use different zones of clocks to reinforce energy run-on wires between the gates to keep the quality of a circuit fan out. The second is using redundancy cells or gates. So, inverter gates are the best option because at the same time can provide two crucial roles. In other words, at the same time, the proposed gate can increase the signal's propagation bandwidth and provide a value generator ability. Regrating the fact that, with the use of even numbers of inverter gates in the line-based structure, an initial logic value can keep it at the end, but when we have odd numbers of inverter gates in the line-based format, in the output cell, we will have reverse values. The same challenges regarding signal driving are available in the pipeline circuit (Almatrood and Singh, 2018). Therefore, the efficient architecture will increase the total efficiency of the whole circuit. Implementing a useful Inverter gate leads to a reduction in complexity, delay, and cell count, particularly in multi-value logic (MVL) designs.

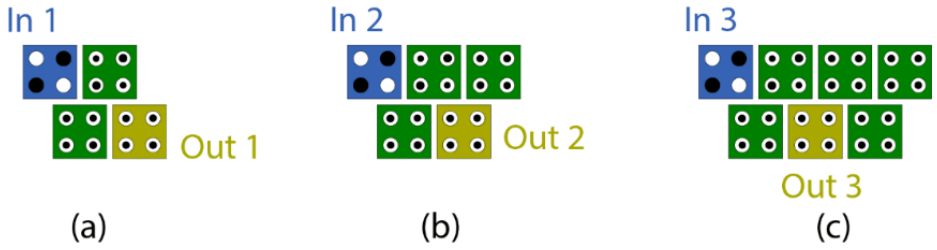

Fig. 6. Proposed inverter blocks in three forms (a) layout 1 (b) layout 2 and (c) layout 3.

In order to clarify the advantages of the proposed design in several level gates, a repeater circuit is constructed because this is a tangible example to show the high-polarization capability of the proposed inverters as depicted in Fig. 7. As a result, proposed repeater structures can be used in various memories to simplify these issues and challenges (Farhadtoosky et al., 2015).

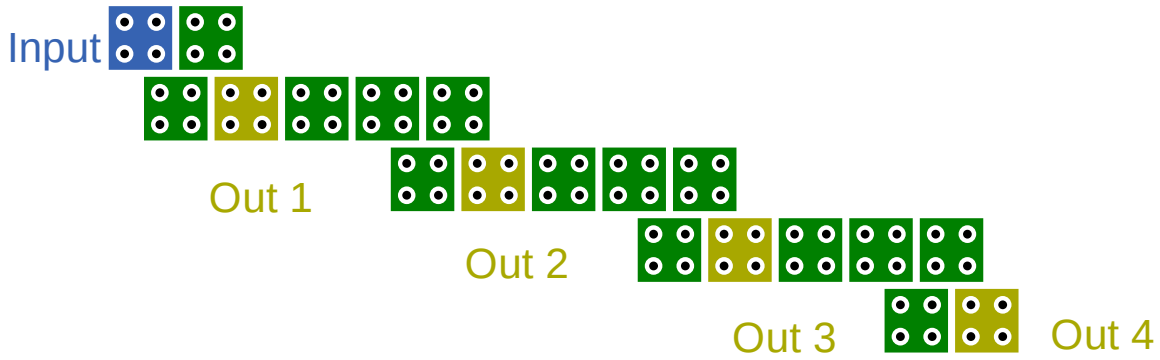

Fig. 7. Proposed Repeater with Four-level output.

5. SIMULATION RESULT AND COMPARISON

In this section, we will discuss the simulation outcomes of the proposed blocks. We utilizes QCADesigner software (Walus et al., 2004) for designing and simulating QCA circuits, which is a widely used tool in this domain. The proposed inverter blocks have low complexity in terms of both cell count and area, and they also exhibit high-level polarization, as demonstrated in the output waveforms illustrated in Fig. 8. The simulation findings indicate that the proposed blocks are error-free and display a noticeable polarization level. The efficiency of the proposed inverters was assessed in terms of three metrics (polarization level relative to temperature, cell count, and area), and the results are presented in Table 1. Furthermore, to better evaluate and compare the inverter gates, their energy consumption are calculated using the QCAPro tool (Srivastava et al., 2011), and the results are given in Table 2. Additionally, the simulation outcomes of the proposed repeater are presented in Fig. 9, which demonstrates a significant polarization level.

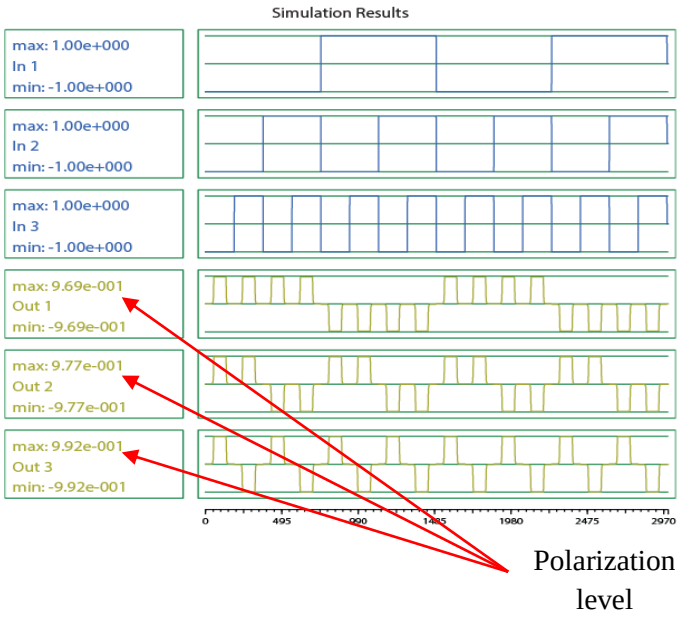

Fig. 8. The output waveforms of the proposed inverter blocks.

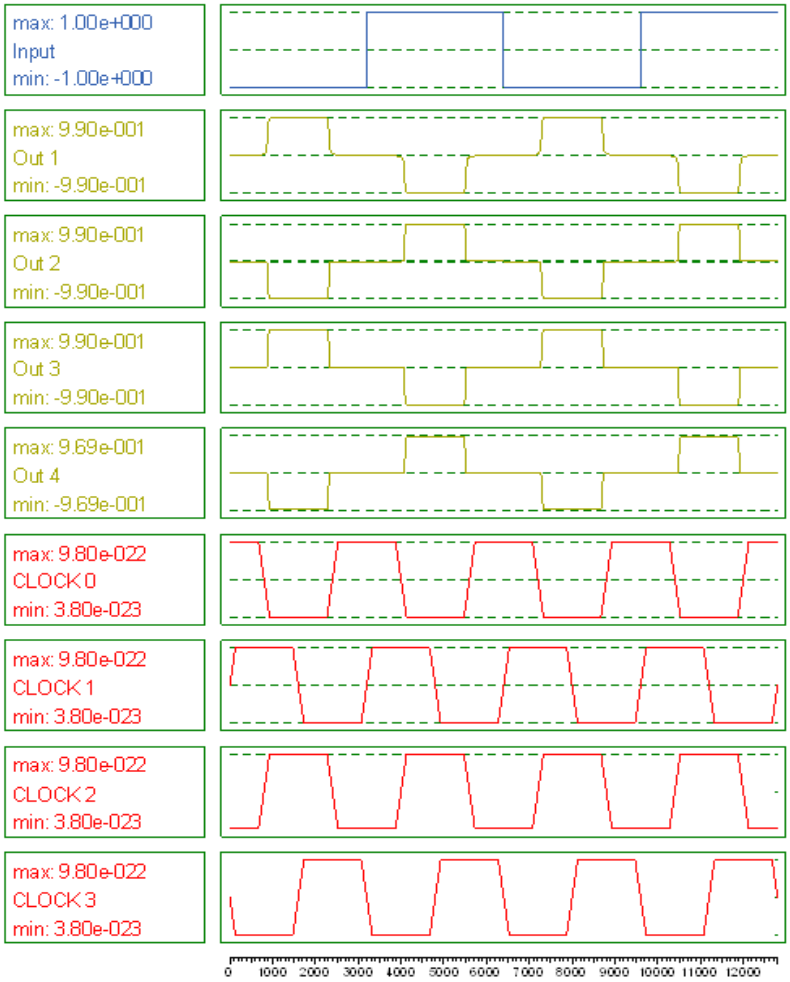

Fig. 9. The output waveforms of the proposed inverter blocks.

Table 1. Inverter blocks polarization over temperature.

Polarization of	Temperature (Kelvin)				Cell count	Area nm^2
	1º	10º	15º	20º		
design in (Tougaw and Lent, 1994)	0.95	0.883	0.668	0.309	4	2964
design in (Tougaw and Lent, 1994)	0.951	0.891	0.706	0.353	9	6844
design in (Kalogeiton et al., 2017)	0.951	0.887	0.672	0.262	9	9604
design in (Kumar and Mitra, 2016)	0.965	0.927	0.761	0.417	9	5684
design in (Goswami et al., 2020)	0.969	0.947	0.876	0.781	6	3364
design in (Goswami et al., 2020)	0.951	0.879	0.635	0.307	6	2964
proposed 1	0.969	0.944	0.842	0.66	4	1824
proposed2	0.977	0.966	0.902	0.769	5	2204
proposed 3	0.992	0.991	0.983	0.947	7	2964

Table 2. Power analysis results of Inverter gates.

	Avg. leakage energy dissipation (meV)			Avg. switching energy dissipation (meV)			Total energy consumption (meV)		
INVs	0.5 E_K	1 E_K	1.5 E_K	0.5 E_K	1 E_K	1.5 E_K	0.5 E_K	1 E_K	1.5 E_K
(Tougaw and Lent, 1994)	0.0019	0.0042	0.0065	0.0006	0.0004	0.0002	0.0026	0.0046	0.0068
(Tougaw and Lent, 1994)	0.0025	0.0072	0.0125	0.0101	0.0085	0.0072	0.0126	0.0158	0.0197
(Kalogeiton et al., 2017)	0.0039	0.0100	0.0162	0.0005	0.0003	0.0002	0.0044	0.0103	0.0165
(Kumar and Mitra, 2016)	0.0033	0.0087	0.0147	0.0100	0.0085	0.0071	0.0133	0.0172	0.0218
(Goswami et al., 2020)	0.0037	0.0092	0.0149	0.0008	0.0006	0.0004	0.0046	0.0099	0.0154
(Khosroshahy et al., 2017)	0.0015	0.0044	0.0076	0.0045	0.0036	0.0028	0.0061	0.0080	0.0104
Proposed 1	0.0018	0.0042	0.0042	0.0008	0.0005	0.0003	0.0027	0.0047	0.0068
Proposed 2	0.0023	0.0054	0.0084	0.0016	0.0011	0.0008	0.0039	0.0065	0.0093
Proposed 3	0.0038	0.0085	0.0130	0.0012	0.0007	0.0005	0.0051	0.0092	0.0136

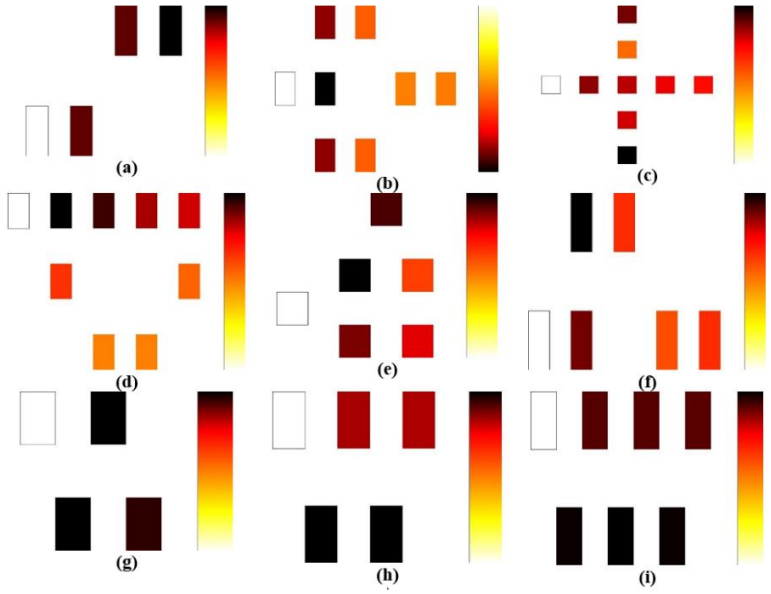

Fig. 10. The power dissipation thermal maps for the QCA Inverter gates at 2oK with Ek (a) (Tougaw and Lent, 1994), (b) (Tougaw and Lent, 1994), (c) (Kalogeiton et al., 2017), (d) (Kumar and Mitra, 2016), (e) (Goswami et al., 2020), (f) (Khosroshahy et al., 2017), (g) Proposed 1, (h) Proposed 2, (i) Proposed 3.

In Table 2, the previous and the proposed designs are evaluated based on three primary parameters: leakage energy, switching energy, and energy consumption in 0.5 E_K, 1 $E_{.K.}$, and 1.5 E_K. Energy level. In addition, in Fig. 10, the thermal maps of circuits are evaluated. In each map, cells with dark colors symbolize high consume energy, and light cell colors mean less

energy consumption in that cell. However, the total energy in each design is aggregate energy in fan out of calls. Hence, the proposed methods have a strong fan out for driving next-level gates. The specification of the proposed repeater gate is presented in Table 3.

Table 3 The Proposed Repeater evaluation with Four-level output.

Repeater	Complexity	Area	Latency	Fixed Value
Proposed	19	0.4	0.25	Not Required

6. CONCLUSION

QCA technology is a new Nanotechnology that has a chance to be a suitable replacement for current CMOS technology. Designing robust and efficient blocks are an essential issue to remain technology in competition. This paper presents three forms of the QCA inverter block. The proposed blocks were built at a low complexity in terms of area and number of cells. The proposed inverter (layout 3) has efficiency improvement by 2%, 4.4%, 11%, and 17.5% over the best-reported inverter block at 10 K, 100 K, 150 K, and 200 K, respectively. Temperature tolerance for the proposed QCA inverters illustrated in the comparison table shows more advantages over others. In addition, we evaluated power consumption and thermal maps of inverter gates. In general, in each circuit design, there is a trade-off between parameters, so in order to gain better fan out energy, we needed to pay much energy. Although, the proposed works' power consumption results compared to most last works could achieve better results. Moreover, this paper introduced an efficient Repeater to show the advantages of output polarization for driving next levels and extendibility. So, the simulation results from output energy levels in the proposed design clearly show better results after applying this method. Besides, this structure is a solution to generate different values for a variety of future circuits.

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