JOURNAL OF KUFA – PHYSICS Vol.1 No.2
A Special Issue for the 2nd Conference of Pure & Applied Sciences (11-12) March 2009

Effect of Different Etching Parameters on Resistivity of Silicon Nano-Material

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Abstract

Silicon nano-material have been prepared in this work via electrochemical (EC) and photoelectrochemical (PEC) etching processes of n and p-type silicon wafers in hydrofluoric (HF) acid of 24.5 % concentration. All conditions preparation such as substrate resistivity, etching time, current density and illumination have been changed to study the effect of these parameters on resistivity of these porous silicon layers.

Introduction

Silicon nano-structure or porous silicon (P-Si) layer is a spongy phase of silicon, uniformly generated by etching process of single-crystal silicon in Hydrofluoric (HF) solutions at moderate current densities. The P-Si structure is characterized by a great number of micropores (2-50 nm in mean diameter), an extremely large surface area to volume ratio and the retention of the crystallinity of original silicon substrates [1]. The discovery of a form of P-Si material with photoluminescence efficiency much higher than that of bulk silicon has led to a flurry of research activity, therefore this material has become popular between scientists and enters in various important applications [2].

Porous silicon layer is mostly fabricated by electrochemical anodization often referred to as electrochemical etching process of bulk silicon wafers in diluted aqueous or ethanoic hydrofluoric acid (HF). Ethanol is often added to facilitate evacuation of Hydrogen bubbles, which develop during the process [3]. Also photo-electrochemical etching process can be used to production P-Si layers which gives advantage of the rectifying nature of the semiconductor/liquid junction; illumination reduces the net etch rate (hole current) at p-type silicon, while it increases the etch rate at n-type silicon [4].

The interest in the electrical properties of P-Si material began prior to the discovery of its efficient luminescence [5]. The material was used for electrical isolation and sensing applications [6]. *Beale et al* [7] have reported that the electrical resistivity in P-Si material is five orders of magnitude higher

than in intrinsic silicon, because P-Si is depleted by free carriers. Depletion can occur either because of the energy gap widening from quantum confinement which reduces the thermal generation of free carriers, or because of trapping of free carriers. Trapping can occur during the preparation of P-Si layer either because the binding energy of dopant impurities are increased or because of the formation of surface states. In this work we have studied the effect of different etching conditions on the resistivity of P-Si layers prepared by EC and PEC etching process.

Experiment

Crystalline wafer of n, p-type Silicon with different resistivities of (12, 3.5 Ω.cm), 508 μm thickness, and (111) orientation was used as starting substrate. The substrate was cut into rectangles with areas of 1 cm^2. The native oxide was cleaned in a mixture of HF and H_2O (1:2). After chemical treatment, 0.1 μm-thick Al layers were deposited, by using an evaporation method, on the backsides of the wafer. Electrochemical (EC) and Photoelectrochemical (PEC) etching processes then performed as shown in figures (1-2) and (2-2).

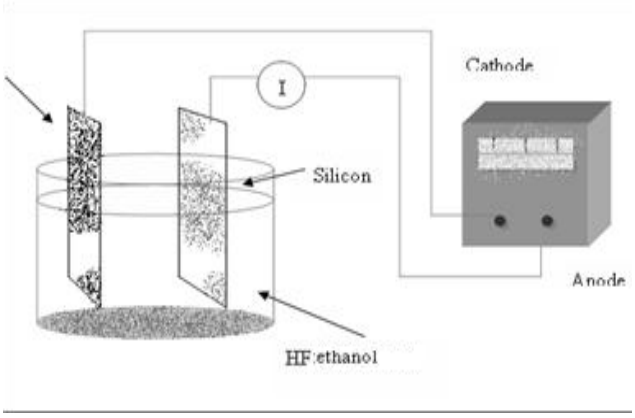

Figure (1-2); The Set-up of electrochemical (EC) etching process.

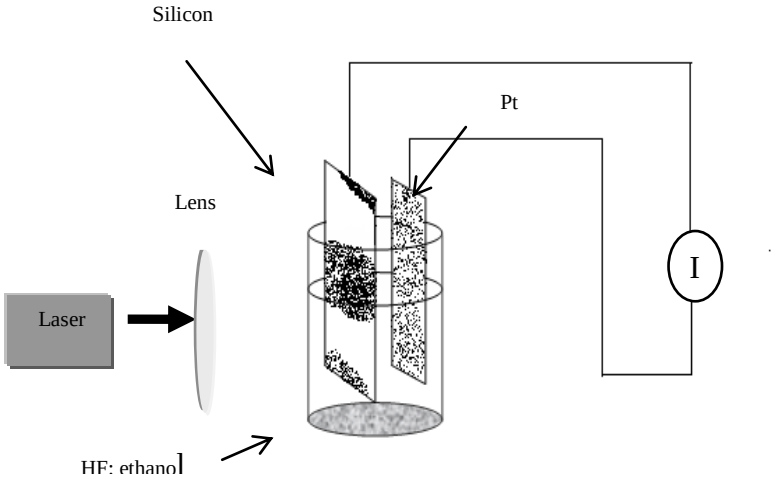

Figure (2-2); The set-up of photoelectrochemical (PEC) etching process.

Both the etching processes have been achieved in an ethanoic solution of 24.5% HF is obtained by 1 volume of ethanol and 1 volume of 49% wt. Hydrofluoric (HF) acid the HF concentration in the ethanoic solution is given by ((1 × 49%)/(1+1) = 24.5%)) (8) at room temperature by using a Pt electrode. The all preparation conditions in this work have been varied such as (conductivity or resistivity of silicon substrates, current density, etching time and illumination).

The resistivity of prepared P-Si layers via both EC and PEC etching processes was accomplished using 4-point probe device which could measure both the silicon types as well as the sheet resistivity. The nanostructure film resistivity was mathematically measured using a simple relation as shown below [9]:

Bulk resistivity (Ω.cm) = Thickness of substrate x Sheet resistivity

Results and Discussion

One of the most principal applications of P-Si material consisting silicon nanocrystallites is the optoelectronic applications based on the efficient electroluminescence. Therefore, it becomes very important to study the electrical properties in order to control the affecting parameters on the electroluminescence [10]. These properties depend strongly on the structural characteristics of the formed P-Si layer especially the surface area and morphology [11,12].

Table (3-1) represents the conductivity type and the resistivity effects on the prepared P-Si resistivity in EC etching process. These samples were formed under similar conditions of 20 mA/cm^2 current density and 24.5 % HF concentration for 60 minutes. One can see that the resistivity increases after etching for all silicon types due to the increase in the path of the carriers with

increasing the disorder of the surface. When a voltage is applied between the two ohmic contacts, current flows through the P-Si layer. We can notice that there is great increase in the resistivity when the doping concentration is high for both n^{++} and p^{++}.

Table (3-2) shows effect of the silicon wafer conductivity on the resistivity of P-Si layers synthesized by EC and PEC etching process. These samples were irradiated with laser of 100 mW power and 514 nm wavelength (made in German) and 24.5% HF concentration for 60 minutes with current density of 20 mA/cm^2.

It is observed that for p-type silicon the resistivity increased from 3.5 Ω.cm to 3.8 with EC etching process, while in PEC etching with the same formation conditions, the resistivity is slightly increased since there was a small modification. For n-type material, the resistivity also is slightly increased from 3.5 Ω.cm to 3.75 Ω.cm with EC etching process, while the illumination effect is much larger which leads to initiate the P-Si layer due to larger number of generated holes. Therefore, a great increase in the P-Si layer resistivity is emerged.

Table (3-1) represents the conductivity type and the resistivity effects on the prepared P-Si resistivity in EC etching process

Conductivity type	ρ_1 (Ω.cm) Bulk Silicon	ρ_2 (Ω.cm) After EC Etching	ρ_3 (Ω.cm) After PEC Etching
p-type	3.5	3.8	3.81
n-type	3.5	3.75	5

Substrate conductivity and the resistivity	ρ_1 (Ω.cm) Bulk Silicon	ρ_2 (Ω.cm) After EC Etching
n-type	11.9	13.75
n^{++}-type	$3*10^{-4}$	3.5
p-type	3	6.4
p^{++}-type	$2*10^{-4}$	2.84

Table (3-2); The effect of conductivity of the silicon substrate on the resistivity of P-Si layers.

We have studied the effect of different etching times on the resistivity of prepared P-Si layers. Figure (3-1) illustrates the relation between resistivity and the etching time for P-Si layers synthesized by EC etching process and PEC etching process with same preparation conditions as in EC etching process.

These samples were irradiated with green laser wavelength of 514 nm on n-type silicon with 3.5 Ω.cm resistivity immersed in 24.5 % acid concentration for various etching times and current density of about 20 mA/cm^2. At the beginning, when we increase the etching time (which is identical to the irradiation time), the P-Si layer resistivity get increased. Due to the resultant large surface area by EC etching process and subsequent increment due to the light absorption in PEC etching process.

As discussed earlier, excessive EC etching occurs for longer etching time (90 minutes) and that is reflected by the sharp decrement in the P-Si resistivity due to the variation in the layer morphology. In this case, the light illumination has greater effect (increase in the resistivity from 3.5 to 5 Ω.cm) and that is because of the light absorption since the band gap here is too small compared to the photon energy. Further increasing the etching times (120 and 150 minutes) leads to form a new P-Si layer with new surface morphology, thus, the P-Si layer resistivity increases from 3.5 to 4.12 and to 5.25 Ω.cm by EC etching process and subsequently to 4.23 and to 6.11 Ω.cm due to the two layers formation and the correspondent large surface area.

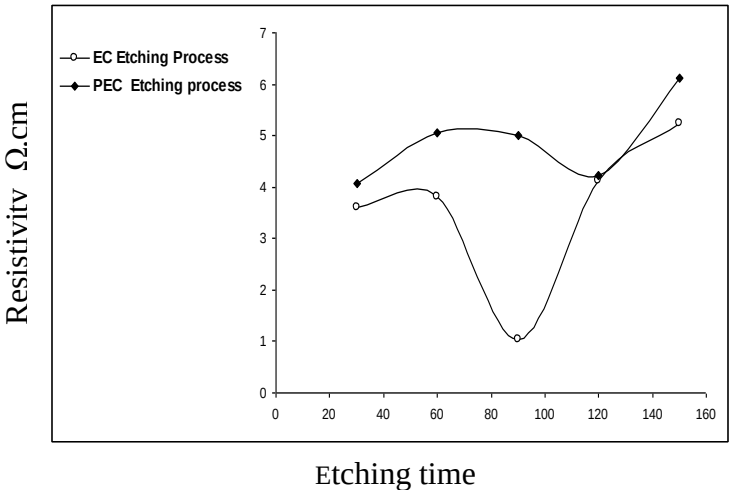

Figure (3-1); The relation between resistivity of prepared P-Si layers and etching time.

We have also studied the effect of different current densities on the resistivity of prepared P-Si layers. Figure (2) shows the relation between resistivity and the applied current densities of P-Si layers synthesized by EC and PEC etching processes for 60 minutes etching time on n-type material with 3.5 Ω.cm resistivity immersed in HF acid of 24.5% concentration and

illuminated with green laser 514 nm wavelength. For 5 mA/cm^2, the two layers produced by PEC etching process have higher resistivity than that of the layer prepared with EC etching process since we have smaller nanocrystallite sizes on the upper layer due to the illumination, which increases the surface area and then, increase the resistivity of the passing current within the P-Si material.

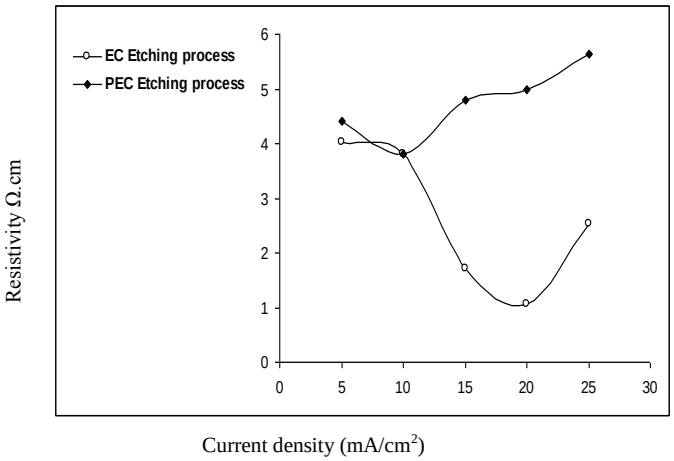

Figure (3-2); The relation between resistivity of prepared P-Si layers and current density.

Similarly, when the current density increased to 10 mA/cm^2, the P-Si layer resistivity increases from 3.5 to 3.8 Ω.cm. Here we can notice that, when the current density increases the etching rate or the etching speed increases. This speed gives no time for the light absorption because the laser induced etching (LIE) is slow and requires a time to generate holes for the etching process.

Therefore, the layer resistivity is almost the same (3.8 Ω.cm) after the EC and PEC etching processes and that means there is no light absorption in this case.

While, the etching process achieve under 15, 20 and 25 mA/cm^2 are inversing at EC and PEC etching processes, where we can notice that the resistivity of prepared P-Si layers by PEC etching process increases with increase of current density, since a good light absorption leads to increase the etching rate which lead to production of two P-Si layers and change the surface morphology of layers. While, we can observed that the resistivity of prepared P-Si layers by EC etching process decreased with increase of current density, because of removal of P-Si layers.

Finally, we have studied the dependence of the prepared P-Si layer resistivity on the illumination wavelengths.

Table (3-3) represents the resistivity of the P-Si layers prepared by EC etching process (ρ_2) and the PEC etching process (ρ_3) for many wavelengths and current density of 20 mA/cm^2 on p-type silicon immersed in 24.5% acid concentration for 60 minutes. Here, we have fixed all the electrochemical parameters so the resistivity will be the same for all samples (3.5 Ω.cm).

With illumination of He-Ne laser of (632.8 nm), small increase in the resistivity of the two P-Si layers appeared due to the small absorption within the first P-Si layer. With decreasing the wavelength to 514 nm, more absorption occurred leading to further etching and increasing the resistivity. By using a blue light of (400 nm) wavelength, higher absorption due to high photon energy leads to increase P-Si layer resistivity. While illumination with white light leads to increase the layer resistivity to a higher value (5 Ω.cm) due to the absorption of all wavelengths constituting the white light.

Conclusion

In light of these results and facts which have been mentioned previously in this work, we can conclude that the preparation conditions have any important effect on electrical resistivity of prepared P-Si layers, where the value of resistivity has been varied with change of these etching parameters and each one of these parameters possess respective effect on this characteristic.

Wavelength (λ nm)	ρ_1 (Ω.cm)	ρ_2 (Ω.cm)	ρ_3 (Ω.cm)
He-Ne laser (632.8)	3.5	3.8	3.811
Diode laser (514)	3.5	3.8	3.85
Halogen light (400)	3.5	3.8	4.125
Wight light (tungsten)	3.5	3.8	5

Table (3-3); The effect of different wavelengths on the resistivity of P-Si layers.

References

[1] Sejoon L. and Deuk Y. Kim, Effect of Incoherent Light Illumination During Electrochemical Anodization on the Formation and the Properties of Porous Si, Journal of the Korean Physical Society, Vol. 47, No. 5., 2005.

[2] Sabah M. Ali Ridha and Oday A. Abbas, Influence of Laser Irradiation Times on Properties of Porous Silicon, Um-Salaama Journal, Girls College of Sciences, University of Baghdad, Vol. 4, No. 4., 2007.

[3] Canham L. T., Properties of porous silicon, Inspec, England, 1998.

[4] Kohl P. A., Photoelectrochemical etching of semiconductors, IBM J. RES. Develop., Vol. 42, No. 5, 1998.

[5] Sabah M. Ali Ridha and Oday A. Abbas, Morphological Aspects of Porous Silicon Prepared by Photo-Electrochemical Etching, Journal of Sciences College, Al-Mustansiriyah University, Vol. 19, No. 1, 2007.

[6] Vincent V. Doan, Reginald M. Penner, and Michael J. Sailor, Enhanced Photoemission from Short-Wavelength Photochemically Etched Porous Silicon, Journal of Physical Chemistry, Vol. 97, No. 17, 1993.

[7] Beale M. I. J., Benjamin J. D., Uren M. J., Chew N. G. and Cullis A. G., An Experiment and Theoretical Study of the Formation and Microstructure of Porous Silicon, Journal of Crystal Growth, Vol. 73, No. 22, 1985.

[8] Feng Z. C. and Tsu R., "Porous silicon", World scientific, London, 1994.

[9] Sze S. M., "Semiconductor Devices-Physics and technology", Wiley, America, 1985.

[10] Canham L.T., Cox T.I., Loni A., Simons A.J., Progress towards silicon optoelectronics using porous silicon technology, Applied Surface Science, Vol. 102, No. 43, 1996.

[11] Ouyang H., Christophersen M., Viard R., Miller L. Benjamin and Fauchet M. Philippe, Macroporous Silicon Microcavities for Macromolecule Detection, Adv. Funct. Mater., Vol. 15, No. 51, 2005.

[12] Jakubowicz J., Study of surface morphology of electrochemically etched n-Si (111) electrodes at different anodic potentials, Cryst. Res. Technol. Vol. 38, No. 3, 2003.

تأثير عوامل القشط المختلفة على المقاومية النوعية لمادة السليكون النانوي

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الخلاصة

تم في هذا البحث تحضير مادة السليكون النانوي التراكيب باستخدام طرق القشط الكهركيميائية والكيميائية-الكهرضوئية لشرائح سليكون ذات توصيلية كهربائية من نوع n و p في حامض الهايدروفلوريك بتركيز 24.5%. عمليات القشط تم انجازها تحت شروط تحضير متغيرة مثل المقاومية النوعية لقواعد السليكون المستخدمة, زمن القشط, كثافة التياروكذلك الاضاءة وذلك لدراسة تأثير هذه العوامل على المقاومية النوعية لطبقات السليكون المسامي المحضرة.