

Design and Implementation of Digital IC Tester Interface to IBM Compatible Computer

تصميم وتنفيذ جهاز اختبار الدوائر المتكاملة الرقمية موصول بالحاسبة الشخصية المتوافقة مع نظام أي بي ام

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Abstract

IC (Integrated Circuit) is important part of electronic circuits, as it has a low cost, small size, high speed, and many other good features. In general, IC's are classified into analogue IC's and digital IC's, the word digital refer that the device can read and write digital signal only which consists of tow levels (logic 0 and logic 1).

This paper discusses the design and implementation of digital IC tester interfaced to IBM compatible computer which enable fast and reliable digital IC testing. Proposed digital IC tester interfaced to computer via parallel port. Device designed to test and analyzes Digital IC behavior in order to verify if it works properly or not.

At many cases, digital IC's must be tested in order to know the damage location in large and complex electronic circuits,

The software that drives the device programmed in visual C++ which enables fast data transmission through parallel port and gives the user the flexibility to test different kind of digital IC's and adds their data sheets to program data base in order to increase software capability.

الخلاصة :

الدوائر المتكاملة تؤدي دورا مهما في تصميم الدوائر الالكترونية وذلك لقلة تكلفتها وصغر حجمها وسرعتها العالية في الاداء بالإضافة إلى العديد من المزايا الأخرى. بشكل عام، الدوائر المتكاملة تصنف إلى دوائر متكاملة مماثلة وأخرى رقمية. إن المقصود بالمصطلح "رقمية" ما هو إلا وصفا للأجهزة التي تقرأ الإشارة بالصيغة الرقمية الثنائية الممثلة ب "0" و "1". يهدف البحث الى تصميم وتنفيذ لجهاز اختبار إلى الدوائر المتكاملة الرقمية موصول ومسيطر عليه بواسطة الحاسبة الشخصية المتوافقة مع نظام شركة أي بي ام . إن المشروع المقترح مربوط إلى الحاسبة الالكترونية عبر المنفذ المتوازي. الوظيفة الرئيسية لهذا الجهاز هو اختبار أداء الدائرة المتكاملة الرقمية واكتشاف نوع وموديل الدائرة . غالبا ما نحتاج إلى فحص الدائرة المتكاملة وذلك لتشخيص الأعطال في الدوائر الالكترونية المعقدة والكبيرة . تمت برمجة البرنامج الذي يدير الجهاز بلغة الفيجوال سي++ والتي تدعم سرعة نقل البيانات والاستجابة مع منافذ الحاسبة الالكترونية . كما أنها تمكن المستخدم من التعامل واختبار مختلف الدوائر المتكاملة باستخدام الجهاز المصمم وخزن قواعد بيانات لخرائط ومواصفات الدوائر المتكاملة الرقمية.

I. Digital IC Tester Design Issues

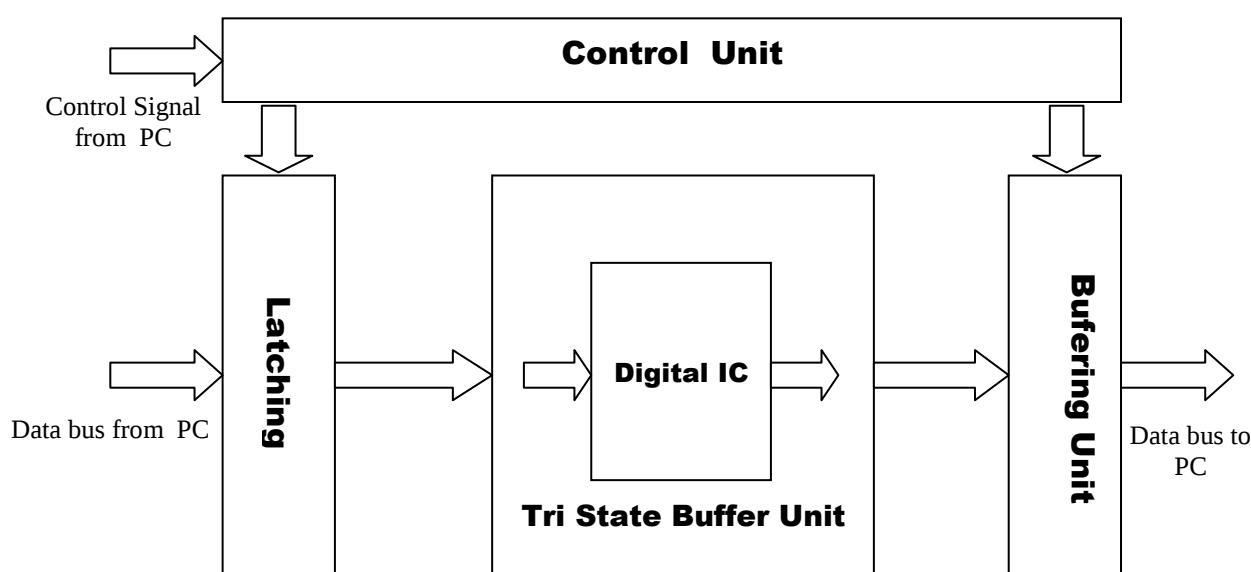
It is important to focus on some parameters related to digital IC tester design, which are:

- 1- It must be compatible with international standard to both of interfaced computer and digital IC.
- 2- Types and size of digital IC that tester capable to test. (Proposed system capable to test both of 14 and 16 pin digital IC).
- 3- Testing speed. How fast to perform digital IC Test.
- 4- Device cost.

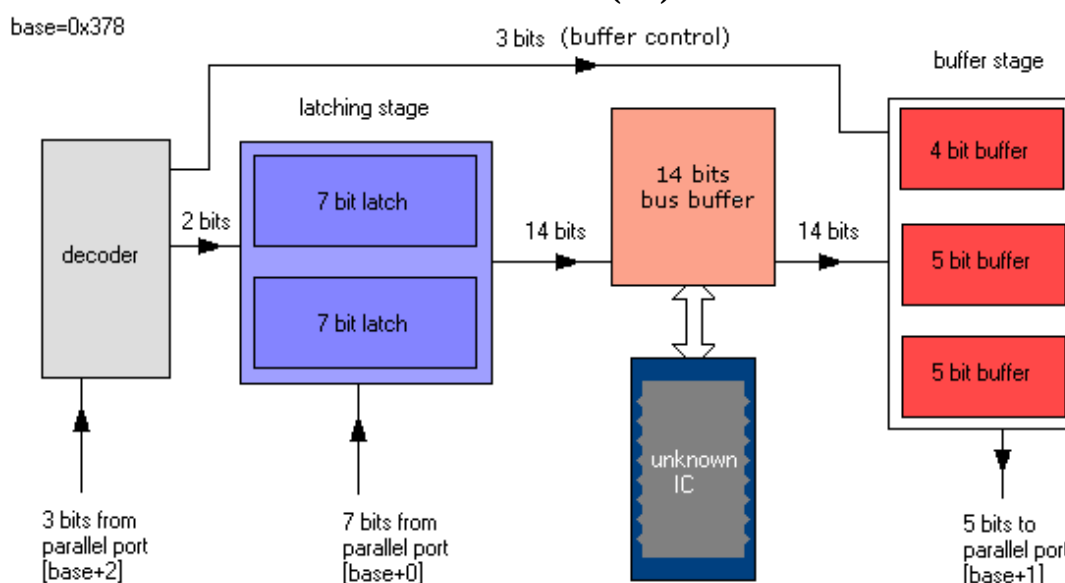
The proposed device in this paper succeeds to reach best rank values for above parameter which make it an excellent solution to those who need to test digital IC's. There are many types of digital IC testers which are usually stand alone testers that did not connected to PC and work alone. Proposed tester in this paper interfaced to PC which leads to best price supported with high compatibility of testing and the ability to add new test to system software by updating interface driver software.

II. Device Hardware Block Diagram

The device consist of many units that works together during IC test, It is responsible of carry testing signals from computer , apply it to IC , read IC response and feedback response to computer for analyzing. Analyzing is done according to predefined datasheets database stored and works beside software. Device units are Decoding unit ,Latching unit , Tri state buffer unit and Buffering unit as shown in figure (1-a) and figure (1-b).



(A)

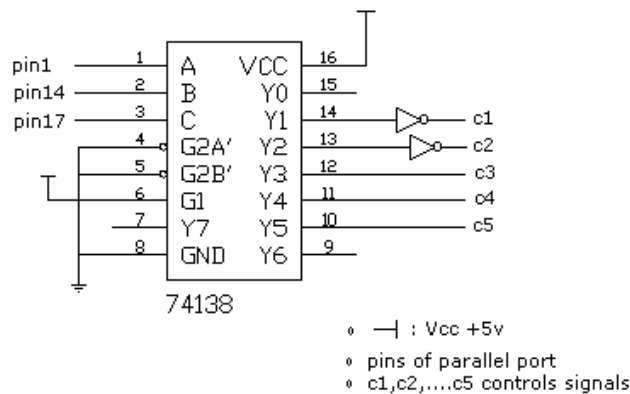


(B)

Figure(1) (A) (B) Block diagram of proposed system interface card

II.I. Decoder Unit

This unit considered as control unit that controlled the data flow to and from IC , it works just like orchestra leader that control latching and buffering unit by sending enabling signals to them. It's feed by control signals from parallel port (base address + 2) via pins 1, 14 & 17 of the 25 pins of parallel port. This unit consist of 3 to 8 decoder (74ls138) which uses to decode 3 lines to 8 control lines . Five output lines from this unit will be used enable signal to control 2 latches and 3 buffers . As shown in figure (2), output lines Y1 and Y2 (C1 & C2) are inverted in order to control latch IC's in latching unit and lines Y3,Y4 and Y5 (C3,C4 and C5) are used to control buffers of buffering unit.



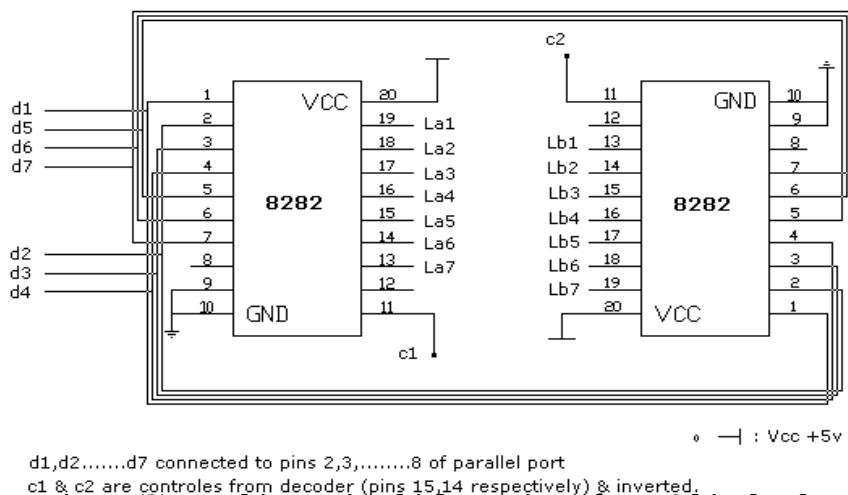
Figure(2) 3To 8 decoder Type (74138) which used to generate control signals

II.II. Device Latch Unit

Parallel Port supports only 8 bit data transmission width via port address (Base+0). Proposed testing device deal with maximum 16 pin digital IC's. So, it needs at least 14 bit data bus (two pins neglected as each digital IC must have at least one VCC and one GND pins which did not need to be connected to data bus rather connected to VCC and Ground directly). Two 8 bit latches (16 bit latching unit) will solve this problem by expanding 8 bit bus into 16 bit (14 bits only will be used).

The latch unit consists of two 8 bit latch IC's type (8282), each of them are connected to bit parallel port bus, the first one activated be C1 control line on order to latch first 8 bit data and the second one will latch the second 8 bit after deactivation of first latch and activate it via C2 control line, by this way we have got 16 bit of data that will be applied to IC.

As shown in fig(3) , the parallel port lines d1,d2,.....d8 are connected to both of latch IC's at the same time both of them are controlled by C1 & C2 lines, the output of both latches are 16 bit bus that will be applied to tested IC.

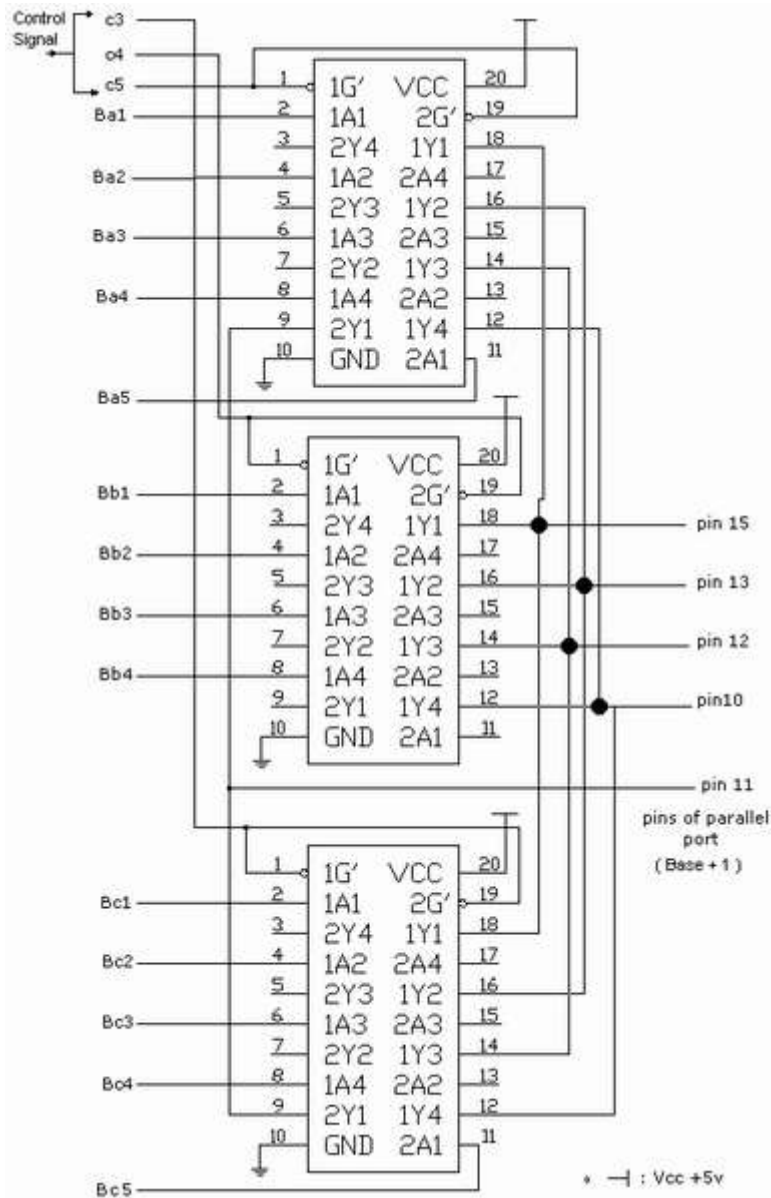


d1,d2,.....d7 connected to pins 2,3,.....8 of parallel port
c1 & c2 are controls from decoder (pins 15,14 respectively) & inverted.

Figure(3) Latching unit which consists of two 8 bits latches type (8282)

II.III Buffering Unit

Parallel port support only 5 bit width input port (Base address+2) over pins no. 10,11,12,13 & 15. In order to read IC response, it must be read at least 14 bit. So, reading process will be separated into three steps, each step will read 5 bits except last step which will read 4 bits (totally 14 bits). This could be done by using three buffers type (74ls244) which controlled via control unit over C3,C4 and C5 control lines as shown in figure (4).



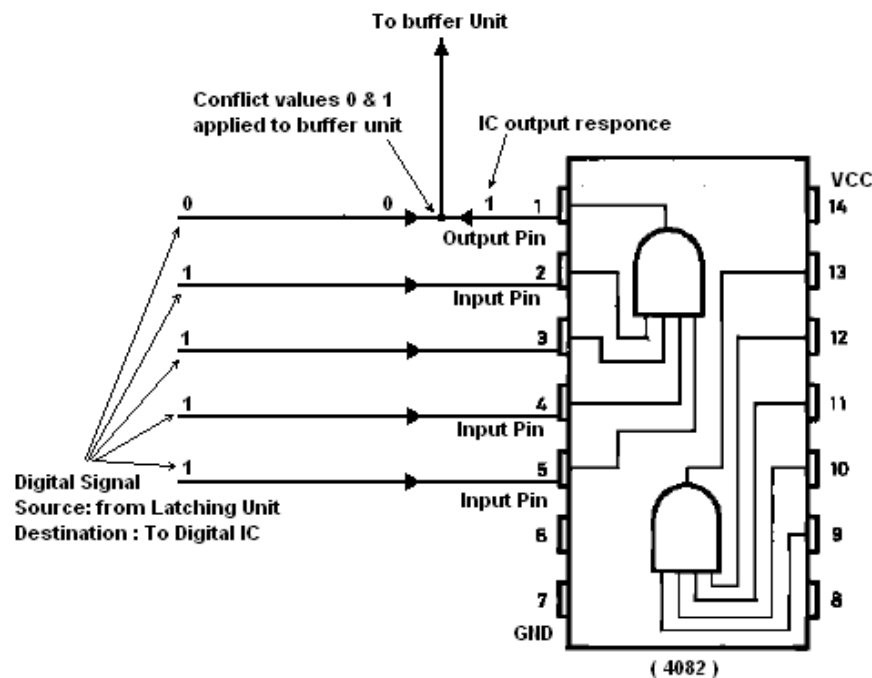
Figure(4) Buffering unit which uses three 8bit buffers type (74ls244)

II.IV. Tri State Buffer Unit

To understand role of tri state buffer unit that is shown in figure (6). It should be discuss the state if it does not exist in device hardware. Buffering unit will be supplied from tow directly connected sources. First is Latches in latching unit and second is digital IC (tested IC) connected to tester. For example, if digital IC type (4082) dual 4 input AND gate tested in device. By applying logic "1" signal to IC pins no. 2,3,4,5 and all other pins set to logic "0". Output pin no. 1 behavior will be logic "1". This will lead to conflict between input signal "0" from latch and output signal "1"

from IC , as shown in figure (5) which lead to incorrect information send to buffering unit. Figure (6) shows the data sheet and logic table of tri-state buffer that is used in project.

To solve this problem, Tri state buffer Type (74ls126) should be inserted between latching unit and digital IC. Tri state buffer will supply two status , logic "1" and Hi-Z (high impedance in order to prevent such conflict between IC latch output and IC output (if it supposed to be output line). Hi-Impedance should be interpreted as logic "0" in case if it supposed to be as an input to digital IC. This could be done by inserting resistance (R) in parallel with tri state output line that connected with digital IC. See figure (7).



Figure(5) If there is no tri state buffer unit . Conflict will be happened in case when Digital IC pin considered as output pin and its logic state "1" while incoming signal from latching unit is "0"

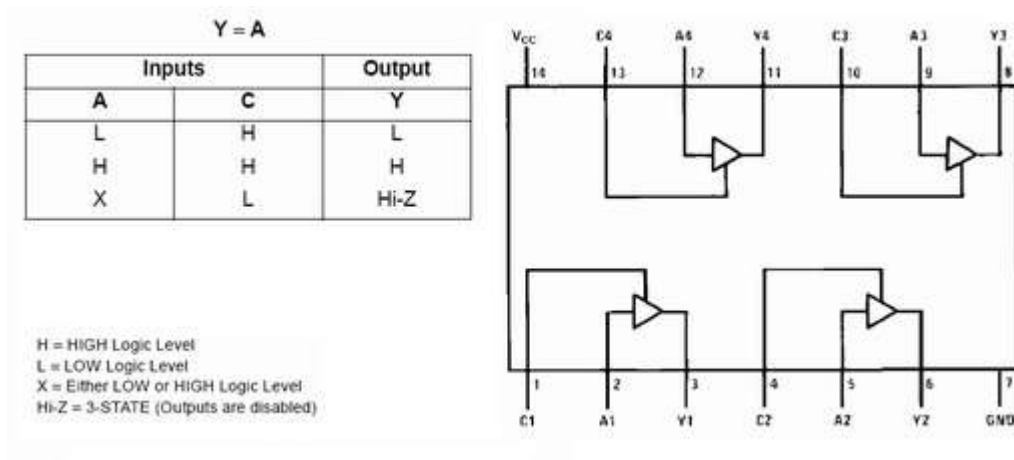


Figure (6) Data sheet and logic table of (74ls126) tri state buffer

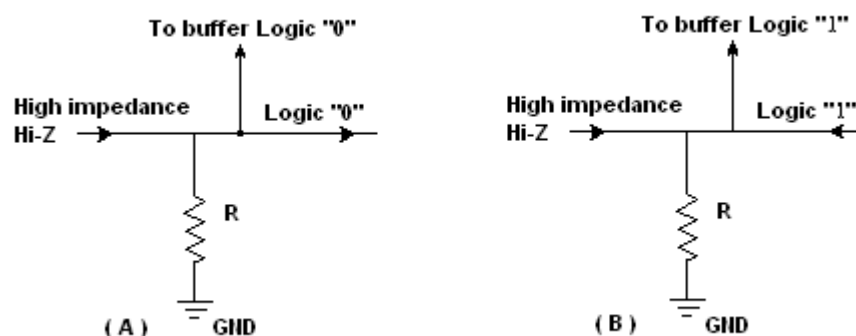
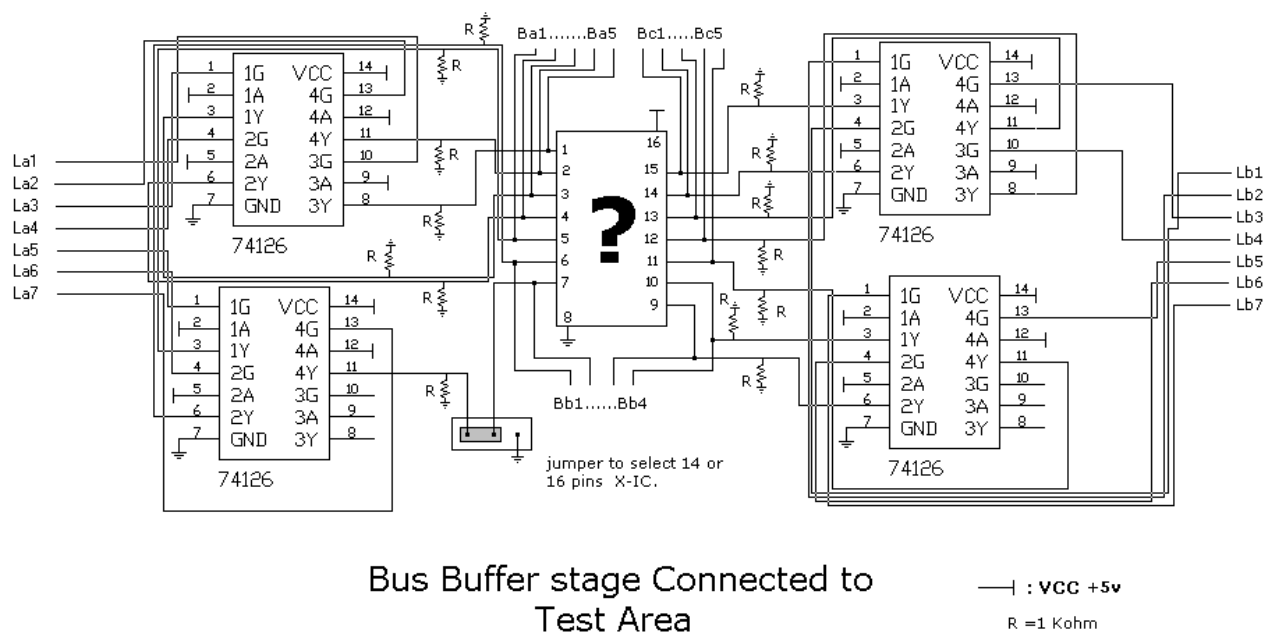


Figure (7) (A) Logic "0" state applied to digital IC. (B) logic "1" response get out from Digital IC (There is no conflict between input line from latching unit and output line from Digital IC as they are separated by tri state buffer)

Final buffer stage unit combined with test socket will be as in figure (8).



Bus Buffer stage Connected to Test Area

Figure (8) Tri state buffers connected to Digital IC

III. Device driver software

In order to operate digital IC tester interface card, Software must be designed to drive it. Software main design issues are :

- 1- Test digital IC manually by sending data signal to IC and read its response.
- 2- Test digital IC automatically according to predefined database of IC datasheets and behavior.
- 3- Contain database modify tool for verifying , edit , add and delete IC behavior according to it's data sheets . This will increase software ability to test various types of digital IC's.
- 4- It should take in considerations standardized rules to be compatible with IBM PC.

IV. Software block diagram

The proposed software designed in C++ . It's block diagram explained in figure (9) which showing main function of software .

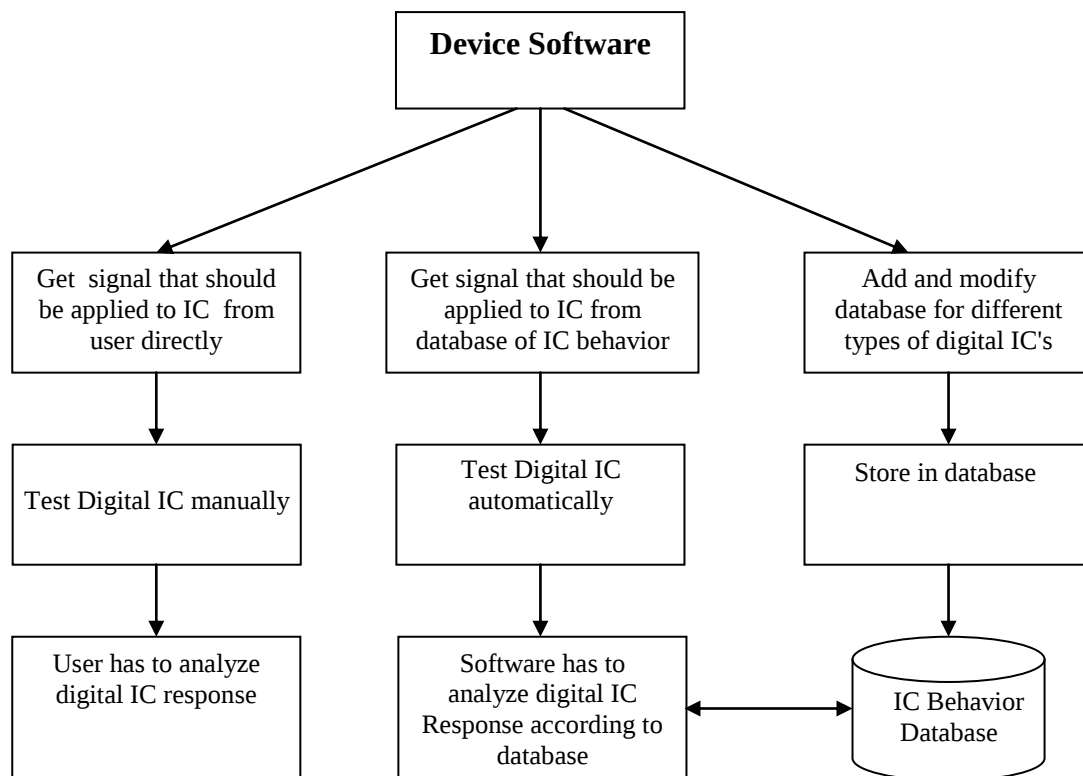


Figure (9) Device Software Block Diagram

Device software consist of three main functions which are : Manual Test which user have to feed signal that should be applied to digital IC manually then analyze it's response according to IC data sheets and IC logic table. Automatic Test which user have to select IC type from menu (IC logic table or IC behavior should be preprogrammed before in system data base) then software will send and receive signal with IC and analyze response according to IC behavior database and Database Tool : This tool enable user to add , remove and modify IC behavior database.

V. Software Operation and User Interface

In main user interface as shown in figure (10) there is simple Integrated circuit diagram that represents the status of real IC. Each IC pin in diagram ended with small circles (red circle represent logic 1 and white circle represent logic 0). Every time we send data to IC. Diagram circles will display IC pins status according to IC response.

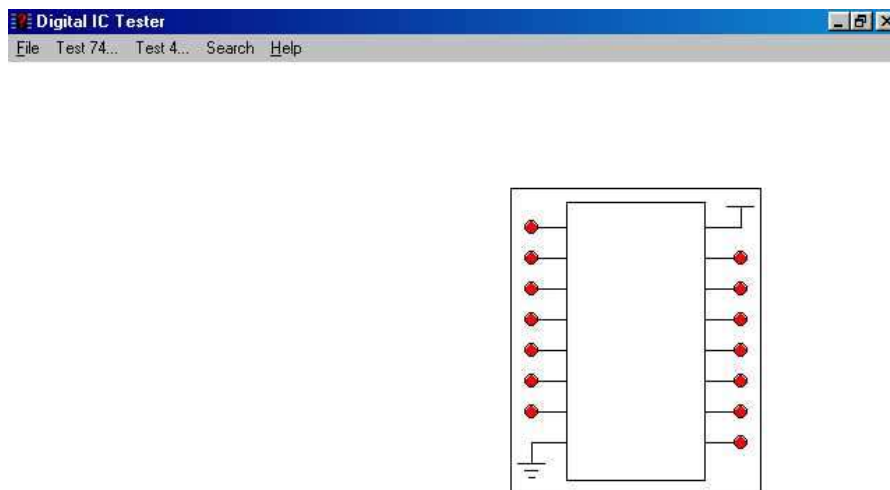


Figure (10) Main User interface of digital IC tester software

In general, software operation is divided into three major parts which are:

1. Manual Test

In this part, digital integrated circuit could be tested manually by opening manual test window as shown in figure (11). Each side of IC consists of two columns of check boxes. The first column is input/output [I/O] column and second one is status [1/0] column. Each IC pin is either input that feeding signal to integrated circuit or output that output IC response. If first column check box selected then it considered that the pin is input to IC then the second column value will force either logic 1 or 0 to that pin according to its status. If the first column checked as output pin then it considered as output, So whatever column two status, the pin will not supply with any signal (high impedance status) and it will be read by interface card as output response of the circuit.

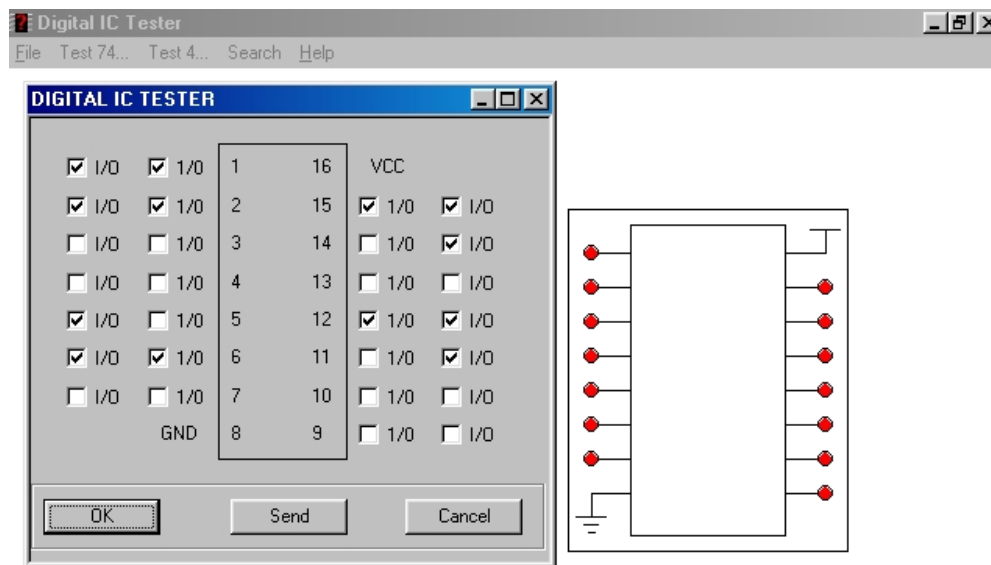


Figure (11) Manual Test Window

2. Automatic Test

In this part, Digital IC could be tested directly by selecting the IC identification No. from test menu then the software will tell through a message box if that IC work properly or not. Test will be done according to previous database stored by programmer contains IC datasheets information and its behavior after applying some of input signals.

For example, after putting IC no. 4066 in Test socket and selecting IC code from automatic test menu. The IC will be tested automatically and test message on figure (12) will be shown after successful test.

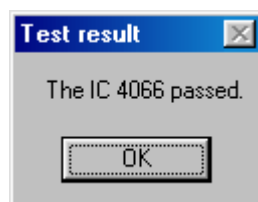


Figure (12) Successful test message

3. IC Auto Search

According to IC datasheets database stored in software, This part allow interface card to discover IC code no. if that IC work properly and its data sheets exists in database .

For example, if software we data base contains the following IC datasheets

(74ls138, 74ls85, 74ls158, 4066 and 4011) the if each IC has been plugged in test socked alone then select automatic search, message box window will appears on screen telling the code no. of tested IC. If plugged IC is not registered in database, text box will appeared telling that such IC is not listed in program list as shoun in figure (13). This function will help in case that technical person needs to know IC code no. of specific IC that does not carry label.

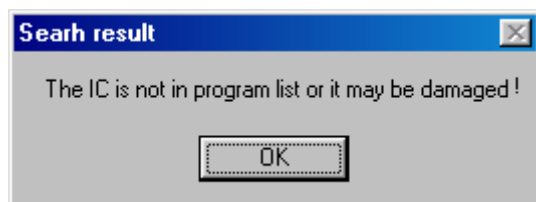


Figure (13) IC not in list message

This means that the IC data base not exists in software database or it may be exists but the IC have being damaged before.

VII. Results and Future works

System design is implemented to interface card and device software are programmed in visual C++. Produced card shown in figure (14)) and it's software have been test successfully by testing and analyzing some samples of digital IC's like 74ls85 (4 bit magnitude comparator) , 74ls138 (3 to 8 Decoder) and 4011 (Quad 2 input NAND Gates). And analysis results give excellent and accurate results.

Future works about to expand card facilities to test analogue IC's by supplying device with Digital To Analogue circuit (DTA) , analogue switches and Analogue To Digital (ATD) circuits. Which enable card to generate and recognize analogue signal and supply it to IBM compatible PC in digital form in order to compare between supplied and received response signal.

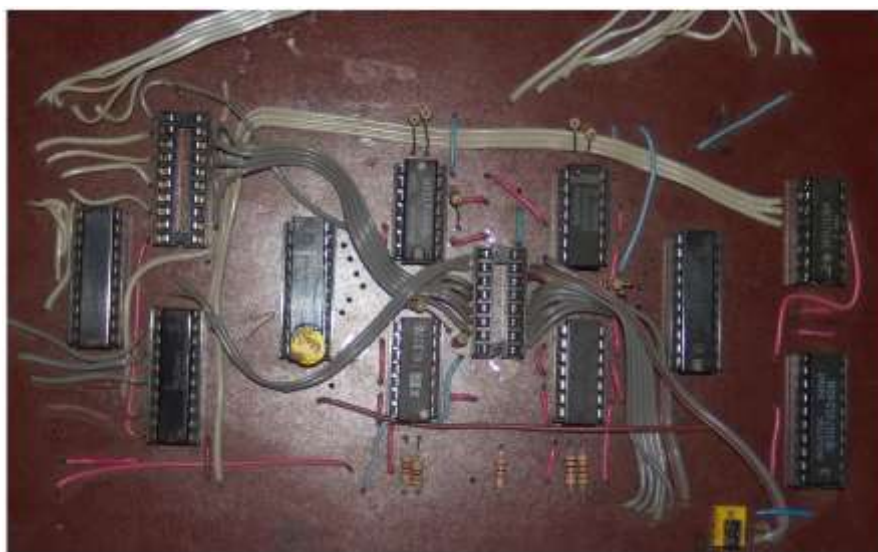


Figure (14) Device Hardware Implementation

Resources

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