Implementation of a Least Mean Square(LMS) Algorithm for Adaptive Channel Equalization using HDL Coder

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Implementation of a Least Mean Square(LMS)..

Abstract:

The LMS algorithm is the most widely used in wireless applications such as equalization and adaptive filtering in imaging, communications, etc. The initialization of the LMS equalizer results from a pilot based channel estimation. This technique is achieved by using algorithms which adapt the coefficients of Finite Impulse Response(FIR) filter to minimize the noise and Intersymbol Interference(ISI) to give an accurate received signal. This paper presents the implementation of the LMS algorithm on Field Programmable Gate Arrays(FPGA). Architecture of adaptive filter that is based on multiplier and adder is to realize the Multiple Access Channel(MAC) operation of the Finite Impulse Response (FIR). The coefficients of the adaptive filter are modified automatically by the LMS algorithm based on input information's. The proposed architecture of this algorithm has been design using Matlab-Simulink (R2015a) to deal with parallel structure. The design has been converted to behavioral VHDL coding style, as will as a VHDL test bench using Simulink HDL Coder tool to realize hardware directly from Simulink design.

Key Words: Adaptive Equalizer, Least Mean Square (LMS) algorithm, field programmable gate array(FPGA) , Finite Impulse Response (FIR) filter.

الخلاصة:

الخوارزمية التكيفية اقل مربع متوسط(LMS)هي الأكثر استخدامًا في التطبيقات اللاسلكية مثل التسوية والفلترة التكيفية في معالجة الصور وهنالك تطبيقات أخرى ، ان التهيئة لمعادل LMS ناتجة عن تخمين القناة القائم على التجربة والاتصالات ويتحقق هذا الأسلوب باستخدام الخوارزميات التي تكيّف معاملات مرشاح(FIR) لتقليل الضوضاء والتداخل لاعطاء إشارة مستلمة دقيقة. في هذا البحث المقترح تم تنفيذ الخوارزمية التكيفية LMS في مصفوفة البوابات المبرمجة رقميا ان بنية المرشح التكييفي الذي يعتمد على المضاعف والأداء في تحقيق تشغيل قناة الوصول المتعدد للاستجابة ذات تم الاندفاع المحدود ويتم تعديل معاملات المرشح التكييفي تلقائيًا بواسطة خوارزمية استنادًا إلى معلومات المدخلات. الى نمط ثم تحويل التصميم Matlab-Simulink (R2015a)باستخدام برنامج المحاكات تصميم البنية المقترحة لهذه الخوارزمية (ترميزالخوارزمية VHDL)

باستخدام أداة لتحول وبناء التصميم مباشرتا باستخدام هذه الأداةSimulink HDL Coder

1.Introduction

Multi-track effect exists in wireless transmission data connection. Signal through different paths of different delays, received at the same time, causing Interfacing between symbols. regrettably most of the time The digital transfer of information is accompanied by A phenomenon known as Intersymbol Interference (ISI).

Transfer information's carrier and peripheral positions (buildings, etc.), produce them spread environmental changes with time. That is, ISI changes caused by many-track effects and time, and I|SI arises when the data transmitted through the channel is dispersive, in which each received pulse is affected some what by adjacent pulses and due to which interference occurs in the transmitted signals. The equalizer is composed of an equalization model and adaptive algorithms. Adaptive algorithms is a technique used to resolve overlapping symbols. Equalization adjustment is used to make the channel attend to an unknown time varying channel, so it needs a special algorithm to update the filter coefficients for channel tracking the changes. Parameters such as: symbol period, propagation delay across multiple paths, Doppler propagation, time of coherence / bandwidth, variable time or fixed property, channel gain etc. Play a pivotal role in the execute a wireless transmissions as summarized in [1].

The paper includes the design and implementation of adaptive equalizer using LMS algorithm.. The target devices are designed and implemented on FPGA. FPGA plays an important function and supply several benefits like prototyping, speed of transfer data,

adaptive, flexibility of structure, rapid execution of calculations and low cost. a group of pipelined devoted processors, is designed as a system of linear variation with integer variables. We demonstrate, how the code-size efficient synthesis on FPGAs can be solved with well-known mathematical programming.

To perform equalization there are various adaptive algorithms can be used[2]:

- Least mean square (LMS)
- Signed LMS -- including sign LMS, signed regressor LMS, and sign-sign LMS
- Normalized LMS
- Variable-step-size LMS
- Recursive least squares (RLS)
- Constant modulus algorithm (CMA)

2. LMS adaptive equalization algorithm

Equalization process is a removal process of ISI and noise effects from the information's, and is located at the end of receiver. The major obstacles to realizing an enhancement digital transfer rates with desired accuracy is intersymbol interference. ISI trouble can be solved using channel equalization [3].The target is to design an equalizer such that the impulse response of the channel/equalizer combination is as close to $z^{-\gamma}$ (delay symbol)may be done. Figure 1 demonstrate a block diagram of such a channel, where d is a delay. Often the channel parameters are not known beforehand and more vary over time, in some applications significantly. And then, it is It is necessary to use adaptive equalizer, which provide means to track channel features.

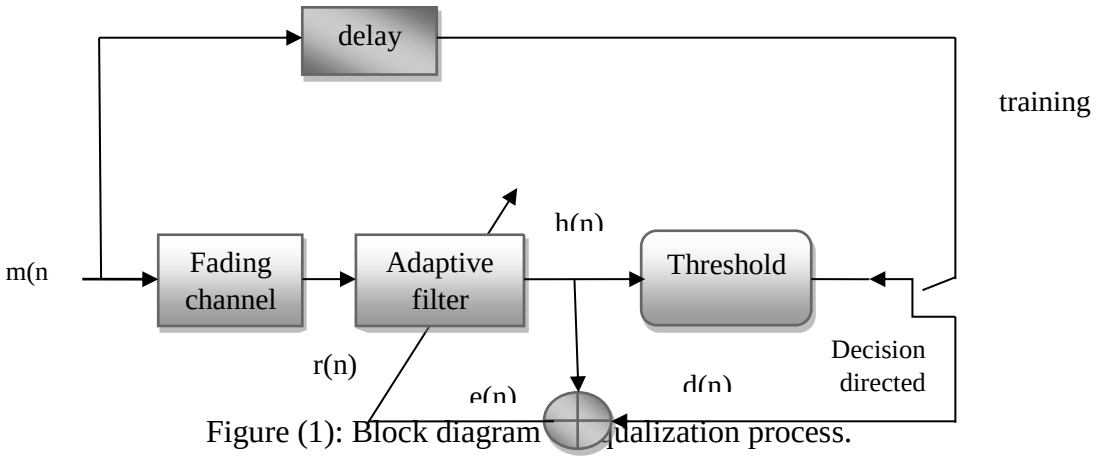

Figure (1): Block diagram of equalization process.

The Fig. 1 shows that the signal m(n) is the signal which send through fading channel and the signal r(n) is considered as the distorted signal through the at the input of filter. The adaptive filter adjust on the value of coefficient of the filter depend on the adaptive algorithm the signal of error e(n) between the adaptive filter output h(n) and desired signal d(n), to compensate for the signal defected, the process of equalization completes by using training data that determine the correct coefficients of adaptive filter and decision directed module can electron switch the adaptive system to decision directed module. At the end the error value e(n) reduced and the coefficients of filter will be similar to the ideal channel[4]. So, filtering process that producing output signals, and training sequence(desired signal)

Figure 2 can be shown the structure of adaptive filter. The data input is the sum of a required data d(n) and interferer symbols w(n)

$d(n) = r(n) - w(n)$ ……..(1)

In the adaptive filtering task, adaptation refers to the method by which the parameters of the system are altred from time index *n* to time index (.*n* + 1).

The structure of variable filter has FIR , the impulse response is equivalent to the coefficients filter. The order of filter is k, and the coefficients are defined such as

$h_n = [h_n(0), h_n(1), h_n(2), \ldots\ldots h_n(k)]^T$……(2)

The symbol error in adaptive algorithm is the difference between the received signal and the estimated signal

$e(n) = d(n) - \hat{d}(n)$……(3)

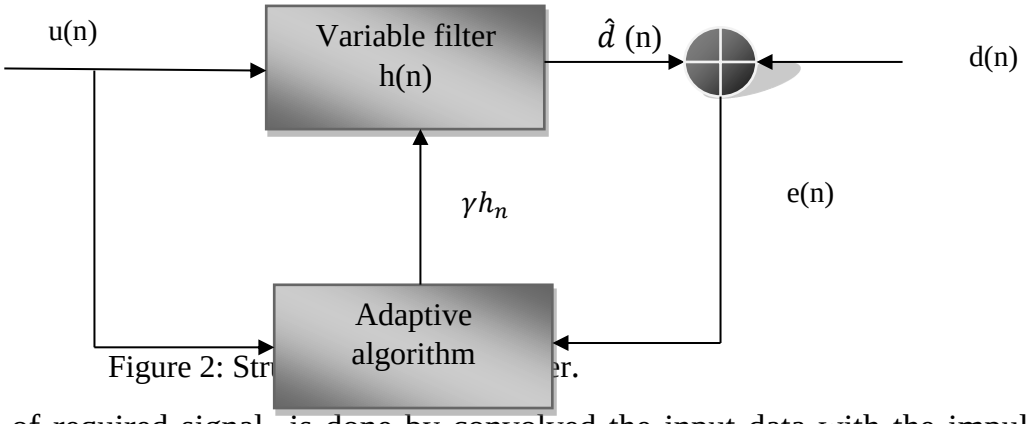

Figure 2: Str er.

The estimation of required signal is done by convolved the input data with the impulse response.

The estimation signal can be expressed as

$\hat{d}(n) = h(n) * r(n)$……..(4)

And input symbols is

$R(n) = [r(n), r(n-1), r(n-2), \ldots\ldots, r(n-k)]^T$……..(5)

R(n)denotes the input signal vector and ·T denotes vector transpose.

For each instant the coefficients of variable filter will be modified

$h_{n+1} = h_n + \gamma h_n$ ……(6)

Where γh_n is a correction coefficient that generated by adaptive algorithm.

The adaptive algorithm uses h_n to updates the equalizer weights. Therefore, the least mean squares (LMS) algorithm searches for the optimum value of filter weights (based on the Minimum Mean square Error MMSE criterion). This process repeated rapidly while the equalizer attempts to converge, and more than one technique (such as gradient or steepest decent algorithms) should be used to reduce the error. At the end, the adaptive algorithm block up the filter weights until the error signal reach to acceptable level or in case of sent a new training sequence [4].The operation modes of adaptive equalizer are training mode and tracking mode.

Implementation of a Least Mean Square(LMS)..

LMS algorithms is consider as a type of adaptive filter utilized to simulate a desired filter by calculate the filter coefficients that contact to producing the least mean squares of the error signal (difference between the desired and the actual signal). It is type of a stochastic gradient descent procedure, which is that filter only updated based on difference between the desired and the actual signal at the current time. Tapped delay line is used to build LMS filter structure which is responsible for performing the filtering process which comprise ,calculating the output d (n- d) of a linear prediction filter in response to the data input and generating an estimation error by comparing this output with a desired response as follows: [5].

$$e(n) = d(n) - y(n) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$$

y (n) is output of filter and demand response at time n.
while the second process of LMS algorithm is adaptive process as mentioned previously which includes the modification automatics the parameter of the filter based on the prediction error.

$$\hat{h}\ (n+1) = \hat{h}\ (n) + \Delta u(n) * e(n) \ldots\ldots\ldots\ldots\ldots (8)$$

Where Δ the step size, and the predicate tape weight vector is (n+1) at time (n+1).So the adaptive filter require (n+1) multiplications and need |(n+1) additions to upgrade the filter weights.
When these both process(filtering and adaptive processes) are working with each other produce the so called feed back loop.

3. Simulink Model of Adaptive Equalizer

Design of Adaptive equalizer can be done using the communications blocks Toolbox which includes Simulink blocks, System objects, and that provide equalization capabilities can be classified as Adaptive or Maximum-Likelihood Sequence Estimation:
Figure 3 shows the SIMULINK model of adaptive equalizer

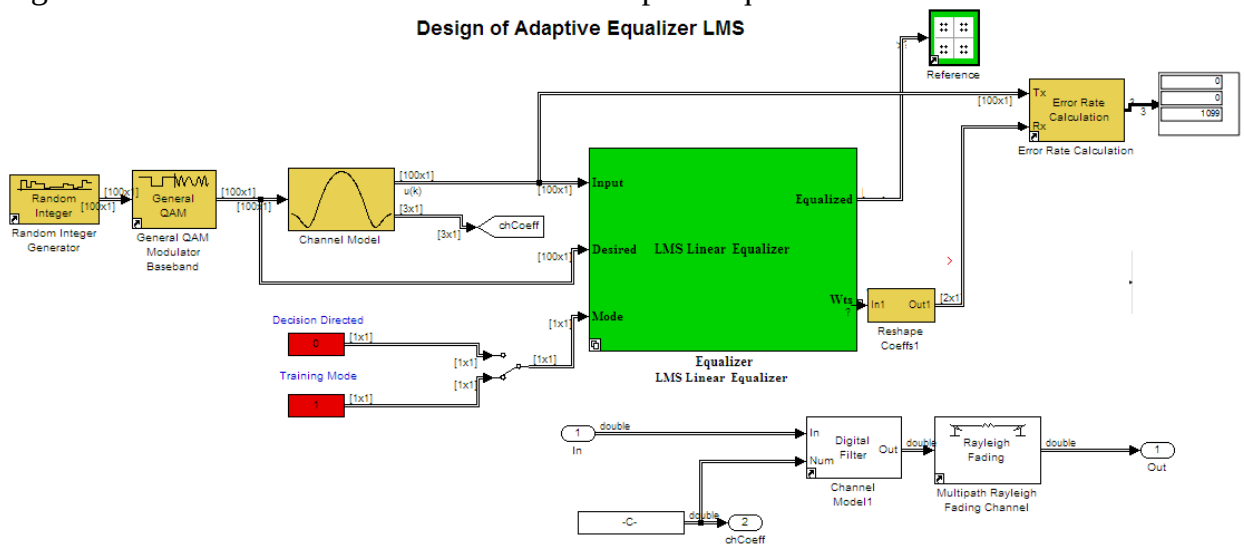

Figure 3: Simulink Model Adaptive Equalizer

Structure of Simulink model comprises of block of generate random integer, MQAM modulator, symbol converter, , and a raised cosine shaping filter at the end of transmitting side, The type of channel that used is Rayleigh fading., adaptive LMS algorithm module, block for converting the integer value to symbols, and the end of model connected an error calculator, all the blocks designed using MATLAB communications tool. A stream

of bits was transmitted by the generator of random integer block r[n] to simulate a message. The r(n) stream of bits was transform into integer data from 0 to M-1 and this operation is done first, then the modulator carry out its function.

By using delay tapes the required response can be obtained after a Appropriate delay which was execute to the adaptive LMS algorithm in the form of a training series Which plays a role in running filter coefficients by Weighting equations of the upgrade LMS algorithm.

The data bits stream set from the equalizer then mapped return from convertor integer to bits and vice versa, and when reach this step can be calculated error rate of the all emulation, an error calculator block was jointed between the transmitter block and the receiver block which compares input data that transmitting with output data from the equalized.

4. Result of system model

The results(error rate) of this model come from divide random pairs of symbols data by the sequence of data input generated from the integer random block, and this result demonstrated in Figure 4.

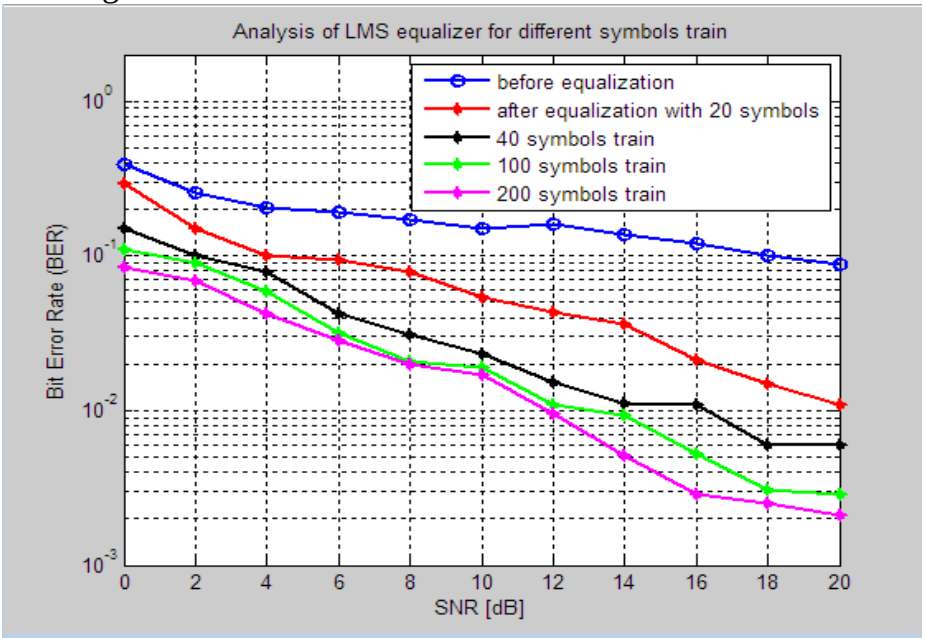

Figure 4: BER for Adaptive LMS Algorithm.

The simulation results shown in Figure 4 demonstrate that performance of adaptive LMS algorithm. Simulated is done in terms of BER and number of errors as a function of differ amount of SNR(dB) with 16 QAM signaling platform, each frame include 2000 symbols(each symbol content four bits) generated by integer block message, over Rayleigh fading channel with doppler shift(fd) equal to = 50 Hz and the other parameters used for algorithm simulations are step size = 0.01, number of filter taps = 6, reference taps= 4, leakage factor = 1. When compare the results that obtained it is clear that performance of the system became better with used adaptive equalizer, and BER for LMS equalizer was improved with the training length is increased from 20 to 100 symbols generated by sequence blocks. Furthermore, it is clear that when training length increased above 100 symbols give rise to reduce efficiency of band width due to high latency, so in this case the BER will be slight improved. Therefore, the distortion that result from ISI effects will be decreased with Adaptive LMS equalizer and limit training sequence.

5. FPGA Implementation results of Adaptive LMS Equalizer

To implement LMS equalizer on FPGA can use Simulink HDL Coder which is high level design tool and faster method which create VHDL code from Simulink blocks and State flow finite state machines, as well as Simulink HDL coder supplies interfaces to collect manually-written HDL codes, HDL mimicry blocks and RAM blocks in its environment[6].

The adaptive LMS equalizer has been designed using Matlab Simulink and tested, also synthesis as well as simulated using Altera Quartus II simulation environment targeting Cyclone III FPGA. It supplies a entire design medium for designing equalizer on a programmable platform. It displays a very substantial library of modules that can be used to build many types of handling units can be used. The designed LMS Equalizer is modular, which gives the planner to check and analysis the different modules separately. Figure (5) shows the block diagram of register transfer level(RTL) of internal structure of the LMS Equalizer. RTL glimmer is used in hardware description languages (HDLs) like VHDL to produce high-level submitting of a system, from which lower-level submitting and eventually active wiring can be obtained, and logic optimization can be obtained by using synthesis tools. Figure (6) shows a schematic file to assign input and output pins for the LMS equalizer system. Finally by using ModelSim Altera 6.1g, can test the signal input and out of all LMS Equalizer and result is shown in Figure (7). The source signal in the simulation can be utilized to compare the result of output signal with input data, the (ce_reult) appears as clock enable. The maximum operating frequency of FPGA implementation is 100MHz and master clock frequency is used 110MHz.

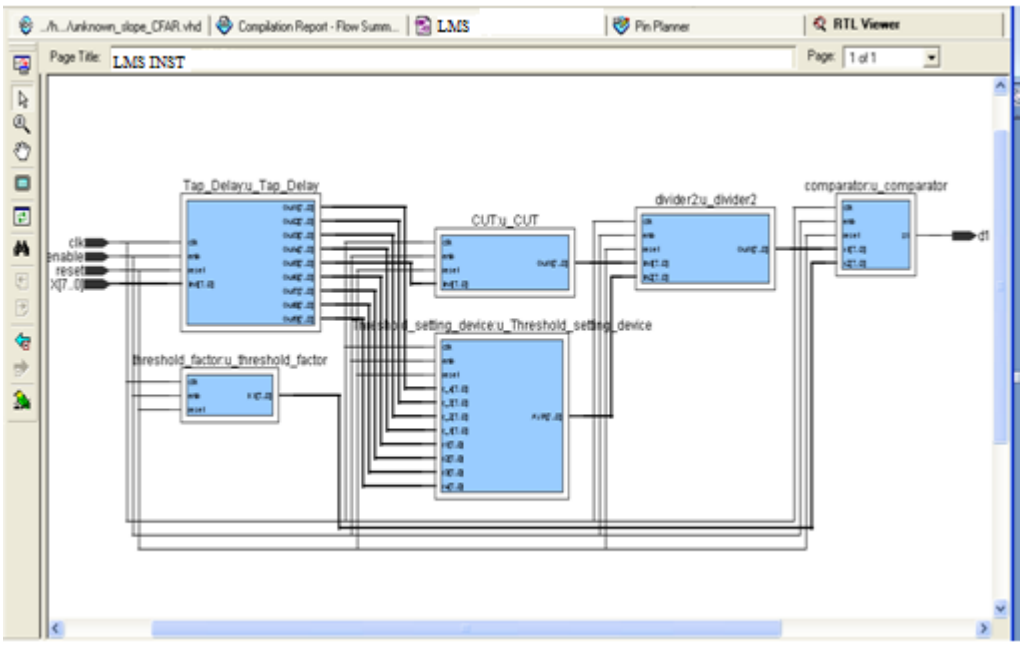

Figure 5**:** Register Transfer Level of Adaptive Equalizer.

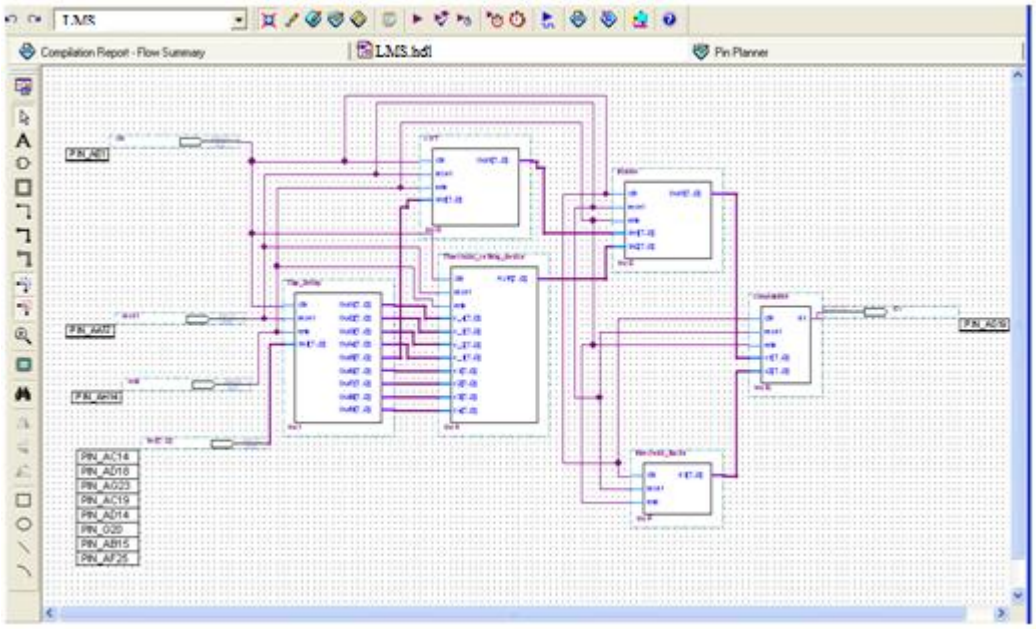

Figure 6**:** Top level design of the Adaptive LMS Equalizer on FPGA Platform.

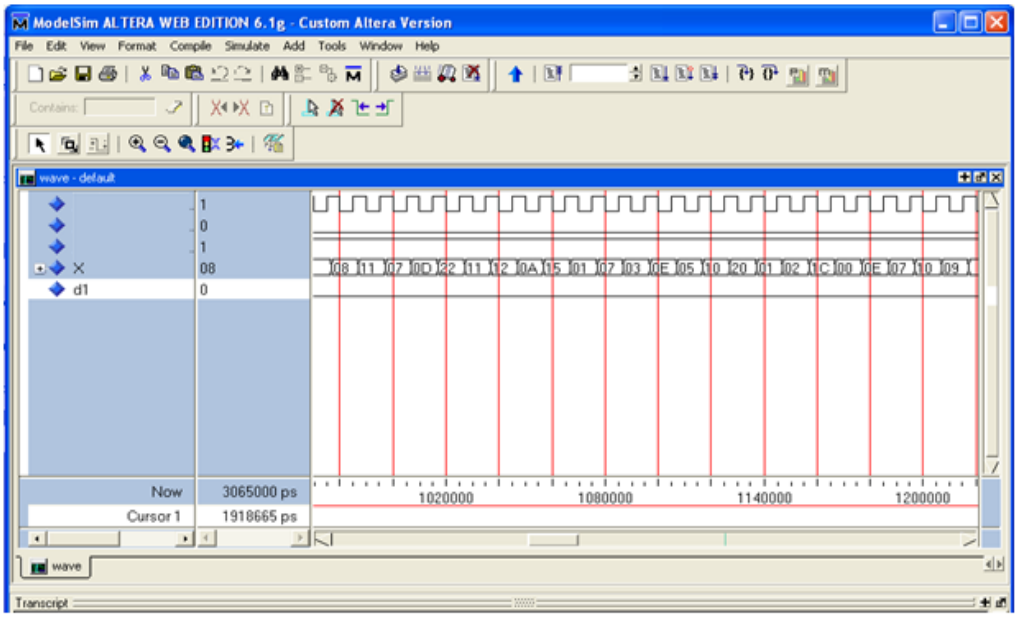

Figure 7: Waveform Simulation of Adaptive LMS Equalizer.

The input clocks that content in the Cyclone III board: 125 MHz, 50 MHz and can add clocks which is consider as external clock by the user. So, the implemented speed must be restricted, when it is implemented on Cyclone III. The synthesis reports for the LMS Equalizer can be summarized as in the Table 1

Table 1: Compilation Summery

The LMS Equalizer Core Synthesis Summary for CycloneIII (EP3C12F780C7) device			
Resources	**Utilized**	**Available**	**Percentage**

Total logic elements	9018	119088	0.7
Total registers	7533	119088	0.6
Total memory bits	6550	3981312	1.6
DSP 9 bit elements	233	576	4

5.Conclusion

Adaptive LMS equalizer in this paper was designed and implemented using Matlab Simulink and FPGA platform, and the response of adaptive filter has been analyzed. Therefore, can be concluded from the simulation results that system has relatively perfect performance in terms BER, when LMS algorithm with FIR filter are used and adapted, where the effects of inter symbol interference result from Time-dispersive channels is minimized . While, the defect of LMS algorithm is that the converge is slow gradually. The implementation of the LMS algorithm is accomplished via field programmable gate array (FPGA) design through create connection link between simulink design and VHDL by using HDL coder tools which simplest and active procedure for control users. The speed, capacity consumed, and complexity are clear in the compilation report, and complexity can be improved by using multiplex multiplier, so the multipliers that used in the implementations can be reduced.

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