DESIGN OF A SOFT CORE BASED WAVELET PACKET TRANSFORM SYSTEM [+]

Mazin Rejab Khalil [*] **Ahmad Kussay Kayali [**]** **Louay Chachati [**]**

Abstract :

Wavelet Packet Transform (WPT) is an effective tool for analyzing signals used in different practical applications especially in speech and image processing fields. This paper introduces a design of a wavelet packet transform system configured on field programmable Gate arrays (FPGAs) slice using embedded design techniques. The hardware part is constituted by configuring a Microblaze soft core processor system on Spartan 3e FPGAs slice. The floating point unit available in the Microblaze processor is enabled to make the system deal with 32 bits floating point numbers as well as integers. A DDR-SDRAM with 64 Mbytes capacity is added to the hardware to accommodate with the signals containing high frequency components, like image signals, that implies large number of samples. The embedded processor system is programmed by a C language application program to make the system act as a wavelet packet transform system. Xilinx ISE10.1 software was utilized to develop the hardware and software parts of the designed embedded system. System performance is tested for seven levels decomposition of an audio signal with satisfactory results obtained compared with the results achieved by Matlab 7.2 version software.

تصميم نظام تحويل حزمة المويجة باستخدام المعالج المصغر ذات النواة المبرمجة

مازن رجب خليل أحمد قصي كيالي لؤي شاشاتي

المستخلص:

يعد نظام تحويل حزمة المويجة من الأدوات الفعالة في تحليل الإشارات الرقمية والذي يستخدم في تطبيقات متعددة مثل معالجة الصور ومعالجة إشارات الصوت وغيرها. يقدم البحث طريقة لتصميم نظام تحويل حزمة المويجة وتنفيذه على البوابات المنطقية القابلة للبرمجة الحقلية باستخدام تقنية التصاميم المطمورة. تم إنشاء الكيان المادي بتصميم نظام للمعالج المصغر ذات النواة المبرمجة نوع Microblaze وملحقاته من الدوائر المحيطية مع تفعيل وحدة الفاصلة العائمة لتمكين النظام من التعامل مع الأرقام الحقيقية المؤلفة من 32 بت مع إضافة ذاكرة وصول عشوائي سعة 64 M byte نوع DDR SDRAM إلى النظام لتمكينه من التعامل مع الإشارات ذات المحتويات الترددية العالية مثل إشارات الصورة التي تحتاج إلى عدد كبير من العينات لتمثيلها. تم برمجة النظام بلغة

[+]Received on 7/6/2012 , Accepted on 24/2/2013 .

[*]Asst. Prof./ Technical College of Mosul

[**] Prof./ Faculty of Electrical and Electronics Engineering. University of Aleppo.

C بتصميم برنامجا تطبيقيا لذات الغرض لجعل النظام يعمل كوحدة لتحويل حزمة الموجية. استخدمت البيئة البرمجية المتكاملة ISE10.1 المعدة من قبل شركة Xilinx في إنشاء الكيان المادي والكيان البرمجي للنظام. تم اختبار مستوى أداء النظام بمقارنة النتائج التي تم تحقيقها لسبعة مستويات من التحليل مع نتائج التحليل التي تحققت باستخدام برمجيات Mat lab .

Introduction :

Wavelet packet transform is a powerful tool that can be used to partition the high frequency side (upper half band) and the low frequency side (lower half band) of signals into smaller bands, besides its ability to segment the frequency, it can make a uniform translation in time[1]. The Wavelet packet transform multi resolution capability made this scheme to have a wide range of applications where signal decomposition is necessary especially in digital signal processing, recognition and verification techniques.

The powerful computational requirements of WPT entails a hardware implementation techniques with efficient performance for real time operation.

Embedded design techniques (EDTs) applied on field Programmable Gate Arrays (FPGAs) provides a suitable implementation Platform for this type of analysis due to its high flexibility and adaptability with the system design requirements[2].

The target of the research is to design a system that can be configured on FPGAs to perform WPT tool using embedded design techniques, the design procedure starts by explaining the theoretical basis of the (WPT), EDTs, system hardware implementation and system software implementation. The system is then tested to verify its functionality by analyzing a certain audio signal and comparing the obtained results with those obtained by using Matlab software.

Wavelet Packet Transform (WPT):

Wavelet packet transform provides a multi resolution tool for analyzing non-stationary signals. The coefficients of WPT can be computed using mallat pyramid algorithm [3]. Based on this algorithm the coefficients of any stage can be calculated using the following iterative convolution equations[3]:

$$C_{j+1}(n) = \sum_m h_0(m-2n)\ C_j(m) \qquad (1)$$

$$d_{j+1}(n) = \sum_m h_1(m-2n)\ C_j(m) \qquad (2)$$

The implementation of equations (1) and (2) is illustrated in figure 1. Where the down pointing arrows denote down sampling by two and the other boxes denote convolution by h(n) or FIR filtering[4].

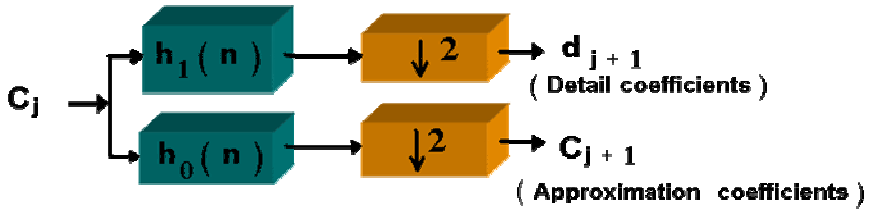


Figure 1. Two Band analysis Bank.

In wavelet packet transform, only the coefficients $h_0(n)$, $h_1(n)$, $C_j(k)$, and $d_j(k)$, in the defining equations (1) and (2) need to be considered, and they can be viewed as FIR digital filters and digital signals respectively. The FIR filter implemented by the transfer function $h_0(n)$ is a low pass filter and the FIR filter implemented by the transfer function $h_1(n)$ is a high pass filter, both filters are half band filters with wavelet based coefficients[4]. Daubechies wavelet type (db7) is selected in this work to be used in the analysis. Table 1. shows the coefficients of transfer function of the low pass and high pass FIR filters based on db7[3]. The number of output samples resulted from convolution is given by,

$$L_0 = L_s + L_f - 1 \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

The number of samples after down sampling is given by,

$$L_d = floor\left(\frac{L_0}{2}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Where L_s, L_f represents the number of samples of the input signal and the filter transfer function respectively, floor is a Matlab function to compute the integer value of a fractional number. The filtering operation with down sampling by 2 is known as a decimation[1].

WPT is the technique in which both approximation and detail coefficients are decomposed repeatedly as shown in Figure 2 which characterizes a three levels WPT system[4]. The number of packets obtained from analyzing a signal using WPT is given by[1],

$$N_c = \sum_{m=0}^{M} 2^m \quad \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

Where Nc represents the number of output packets, m represents the number of the analysis level and M represents the total number of analysis levels. The number of packets in each level is 2^m.

Table 1. The coefficients of the low and high pass FIR filters transfer functions (h_0, h_1) based on wavelet db7

n	0	1	2	3	4	5	6	7	8	9	10	11	12	13
$h_0(n)$	0.0004	-0.0018	0.0004	0.0126	-0.0166	-0.380	0.0806	0.0713	-0.2240	- 0.1439	0.4698	0.7291	0.3965	0.0779
$h_1(n)$	-0.0779	0.3965	-0.7291	0.4698	0.1439	-0.2240	-0.0713	0.0806	0.380	-0.0166	0.0126	0.0004	0.0018	0.0004

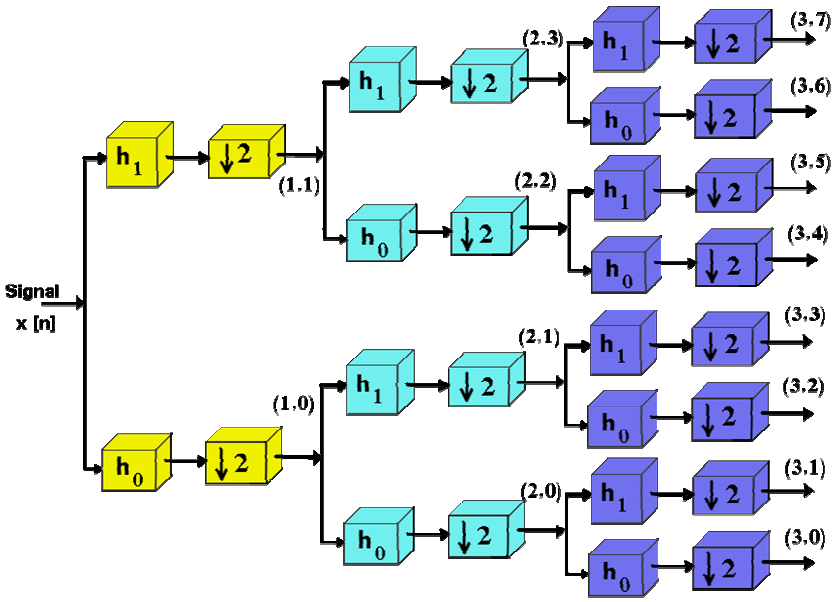


Figure 2. Three levels WPT system.

Embedded Design Techniques :

WPT systems consist of a number of FIR digital filters as shown in figure 2. As the decomposition levels increase, the number of the required digital filters increase accordingly resulting in higher consumption of slice area. This problem is solved using distributed arithmetic and reusing the available resources and modules[5,6], yet this causes other problems to arise as packet tracking. Embedded design techniques represents the suitable solution. EDT helps the designer to configure a processor system on FPGAs. The embedded processor system consists of two parts, hardware part and software part. The hardware part includes the processor, soft core or hard processor, buses, memories and interfacing circuits with peripherals. The software part includes the application program, compiler and libraries. Both parts are transferred into bit files, combined together and configured on the FPGA slice to make the embedded designed system act according to the target. Figure 3. displays the philosophy of the embedded designed systems. The system hardware components are described in microprocessor hardware specification (MHS) file which is introduced with microprocessor peripheral definition (MPD) file to the platform generator which produces corresponding VHDL files that can be applied to the synthesis and following stages. The IP library includes the type of operating system, PCore files implying the available used cores, MPD and microprocessor driver definition (MDD) files.

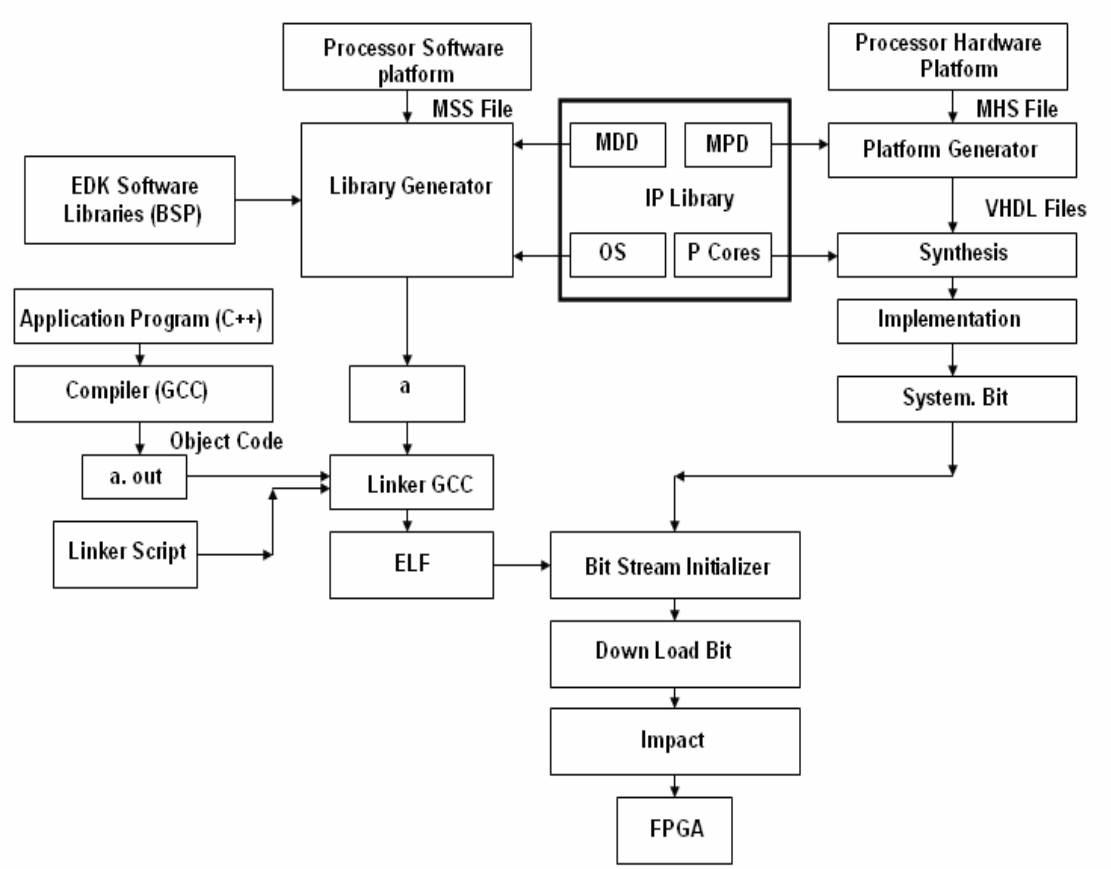


Figure 3. Embedded design techniques.

The software components are described in the software specification (MSS) file which constitutes with library generation and the application program, written in C language, the software part of the system. The hardware part is transferred, according to ISE design flow, into bit file known as System. Bit; while the software part is transferred into bit file known as executable and linkable file (ELF), both bit files are downloaded into the FPGA slice using impact program[7]. The integrated software environment (ISE 10.1) supplied by Xilinx company is used to develop the embedded processor system in this work, it includes embedded development kit (EDK) to construct the hardware part of the system and software development kit (SDK) to raise the software part of the system.

System Hardware :

The hardware part of the system is developed using EDK according to the block diagram shown in figure 4. It consists of Microblaze soft core processor with enabled floating point unit to deal with 32 bits floating point numbers[8], processor local bus (PLB) version 4.6 which is connected to the processor via data interface circuit (DPLB interface) and instruction interface circuit (IPLB interface)[9], interfacing circuit (multi port memory controller MPMC) with a 64Mbytes dual data rate synchronous dynamic RAM (DDR SDRAM) which is necessary to enable the system to deal with high frequency signals which contains large number of samples[10], interfacing circuit (multi channel external memory controller MCH-EMC) with a 16Mbytes parallel NOR flash PROM[11], Uartlite interfaces with RS232 DCE and DTE terminals to input and output data to and out of the system[12],

interfacing circuit to general purpose input/output port(gpio) for 8 bits parallel data[13], interfacing with timer circuit[14], interfacing with interrupt controller[15] and interfacing with microprocessor debug module (mdm). The processor is also connected to a block RAM which is used as a boot memory via local data and instruction memory bus(ilmb, dlmb)[16]. Each of the above hardware components are configured in the form of intellectual property (IP) and their parameters are customized in Xilinx platform studio (XPS) to conform with the designed system targets. Figure 5. shows the assembly view of the system hardware generated in XPS.

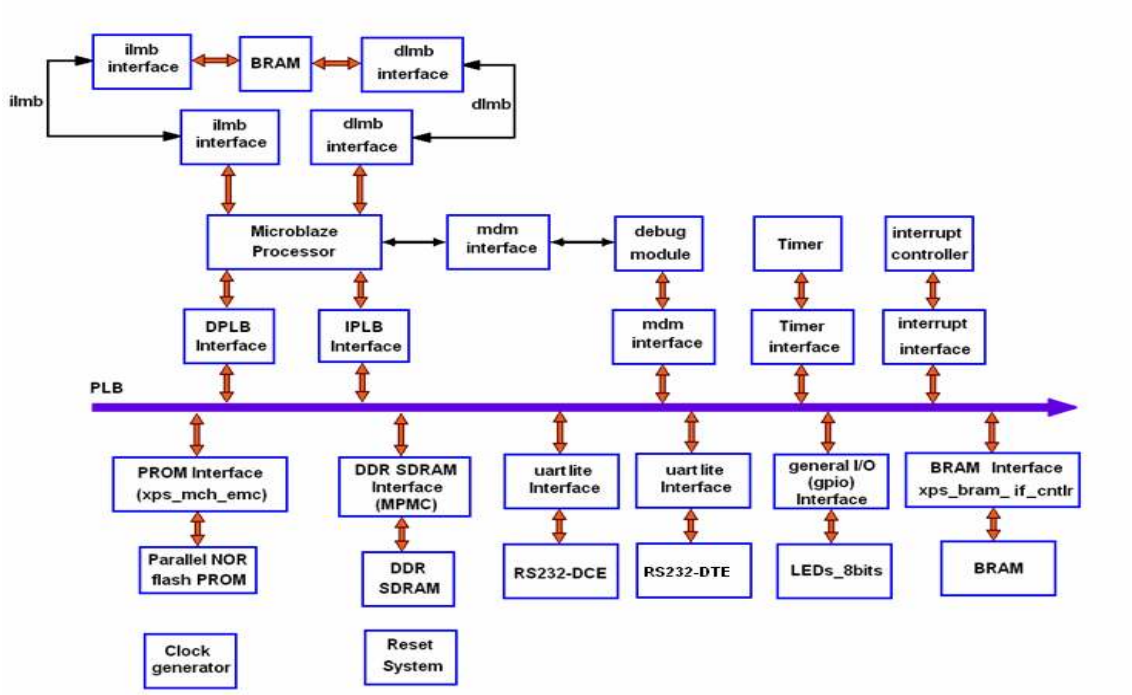


Figure 4. The hardware part of the system

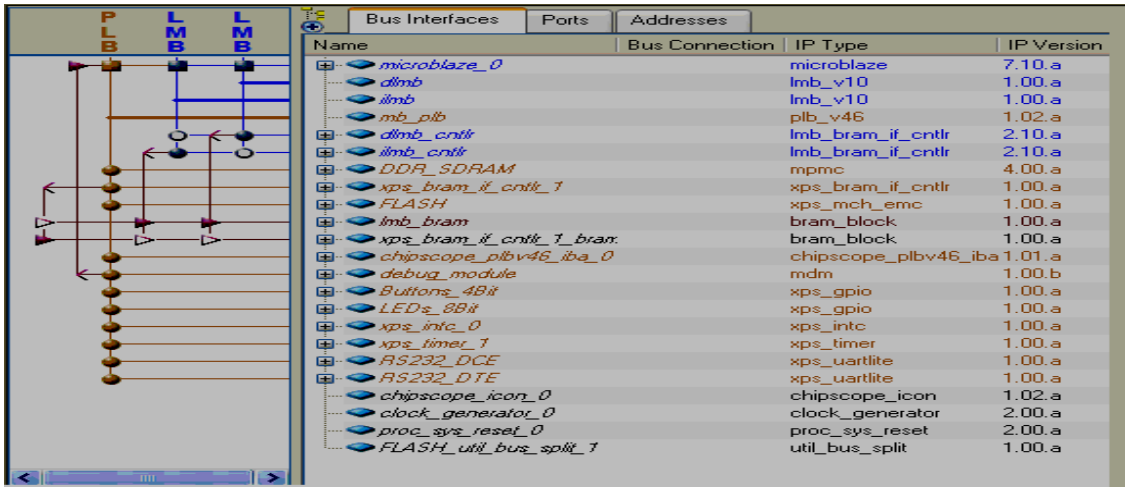


Figure 5. The assembly view of the system hardware generated in XPS

Software WPT Application Program :

The software application program is developed in SDK, it is responsible for making the embedded designed system act as a wavelet packet transform kit. The application program is written in C language to perform a multi resolution analysis on the input signal using WPT technique. The flowchart of the application program is shown in figure 6. Stage(1) represents converting analogue audio signal into digital signal , stage (2) represents the WPT operation and stage(3) represents the application of the analyzed signal. The following steps reveal the principles of the program operations:

1- The signal processing technique depends on executing the convolution equations (1) and (2) between the array [x] which contains the samples of the input signal to be analyzed and the transfer functions of the low and high pass FIR filters (h_0,h_1) shown in table 1. Down sampling by 2 is performed on the output samples of each FIR filter in coincidence with convolution operation by selecting either even or odd numbered output samples. If the number of the input signal samples is 4000, the output samples of the first step of analysis according to equations (3) and (4) is 2007*2=4014 samples.

2- The result of step .1 is stored in the array [x] instead of using two more arrays for the output of the two filters to save memory. This procedure entails adding more fourteen locations to the size of the array [x]. This is performed by shifting each sample in the array [x] fourteen locations to the right. Dummy variables (y0, y) are used to store the temporary values of each output sample of the low and high pass FIR filters respectively, the values of y0 and y are then transferred to the array [x].

3- Shifting the samples in [x] fourteen locations to the right will offer void locations in [x] to be exploited in saving the first seven output samples of each convolution step without losing necessary input data, elements of the array [x] are filled with output samples step by step to the right, the resulting samples of the details and approximation will be stored in the even and odd locations of [x] respectively. The number of output samples in each packet in a certain level of decomposition is calculated by using equation 4. Successive shifting operations with each packet calculations will result in inflating the dimension of [x] to (1*5632) for seven levels analysis.

4- Isolate the approximation and details samples after the first decomposition level by locating the approximation samples to the left of [x] and the details samples to the right of [x] as follows,

[x] = [packet(1,0) , packet(1,1)] ……(6)

5- Apply the above four steps on each packet of equation 6. for second level decomposition. Equation 6. will be given in the following form,

[x] = [Packet (2,0), Packet (2,1), Packet (2,2), Packet (2,3)] ……(7)

6- Apply the first four steps on each packet for different decomposition levels, if seven levels decomposition is performed, the array [x] will be in the following form,

[x]= [Packet (7, 0), Packet (7, 1), - - - - -, Packet (7 , 127)] …….. (8)

7- The variables shown in the flow chart are

n = size of the filter transfer function array.

ss, fs = starting sample, final sample, it is the number of the sample at which the analysis of each packet starts and stops respectively.

m, m0 = the number of samples in a packet before and after convolution operation respectively.
b = the number of packets in each level of decomposition.
ndl = the number of the required decomposition levels.
kk = dummy variable used to represent the number of a packet.
xx = dummy variable used to detect if m0 is odd or even.
sv = dummy variable used to transfer numbers into integers in order to display it on hyper terminal window.

Results :

Audio signals with different numbers of samples are analyzed at different decomposition levels using the designed embedded system, the obtained results are compared with those obtained by decomposing the same signal using Matlab software . Figure 7.a. shows the result of analyzing the first 500 samples of an audio signal, packet(2,0), by the designed embedded WPT system displayed on the window of the integrated bus analyzer (IBA) of Chipscope analyzer, the output samples are gathered during the write phase of PLB. Figure 7.b. shows the results of analyzing the same signal using wavelet tool box in Matlab software. Figure 8. displays packet(3,6) for the selected audio signal on chipscope window compared with that on Matlab window. Figure 9. exhibits the waveform of selected packets at different levels of decomposition, drawn according to the sample values calculated by the designed embedded system and the sample values calculated by the Matlab software simultaneously. The percentage error is 0.03% which indicates the precision of the designed embedded system.

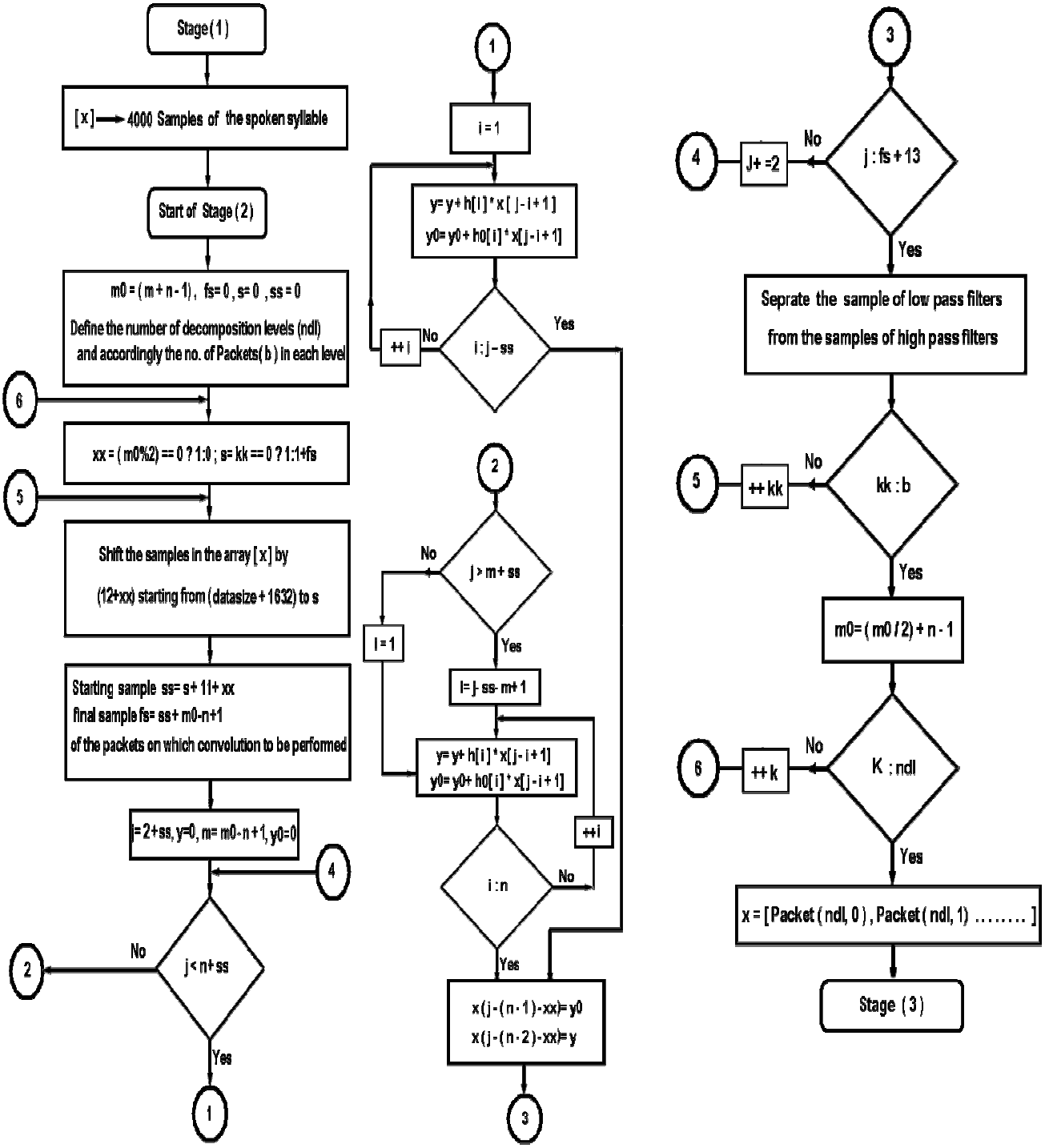
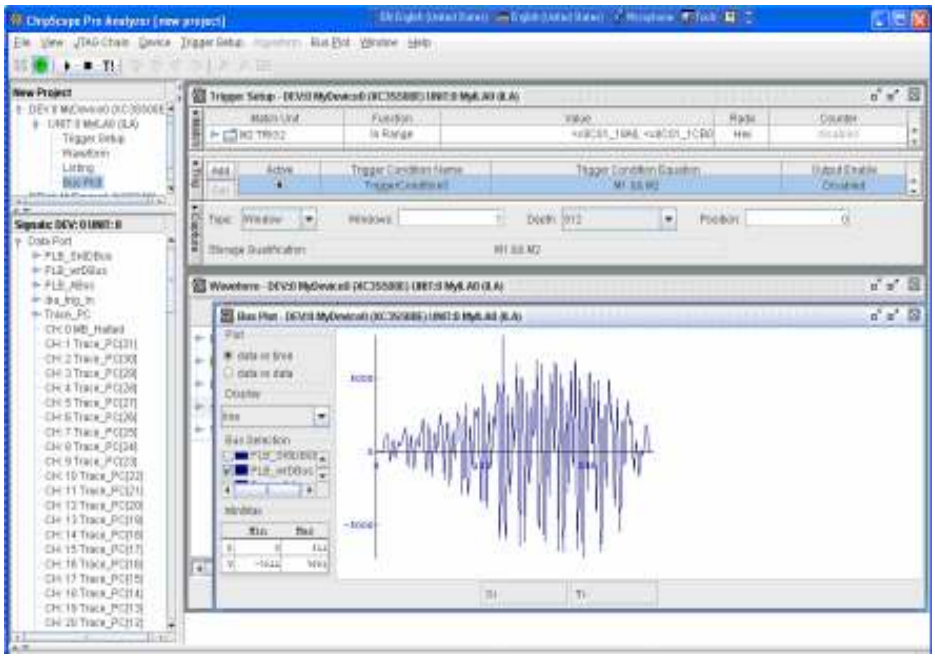
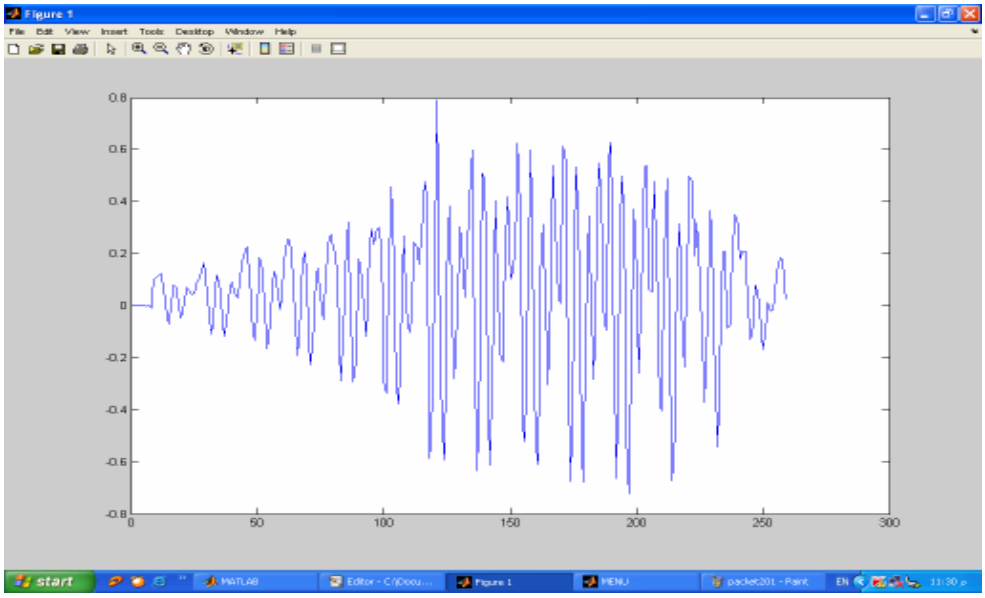


Figure 6. The flow chart of the WPT application program

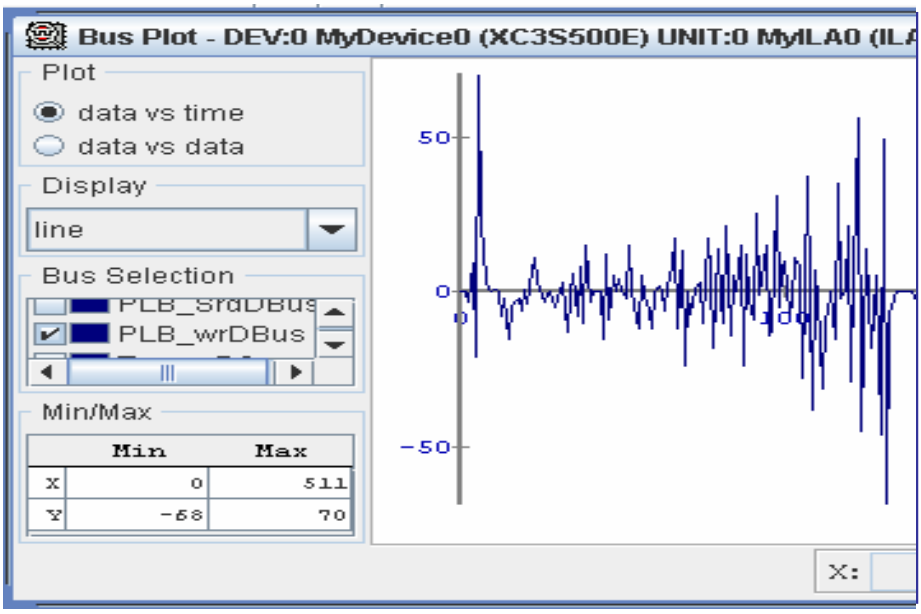


a

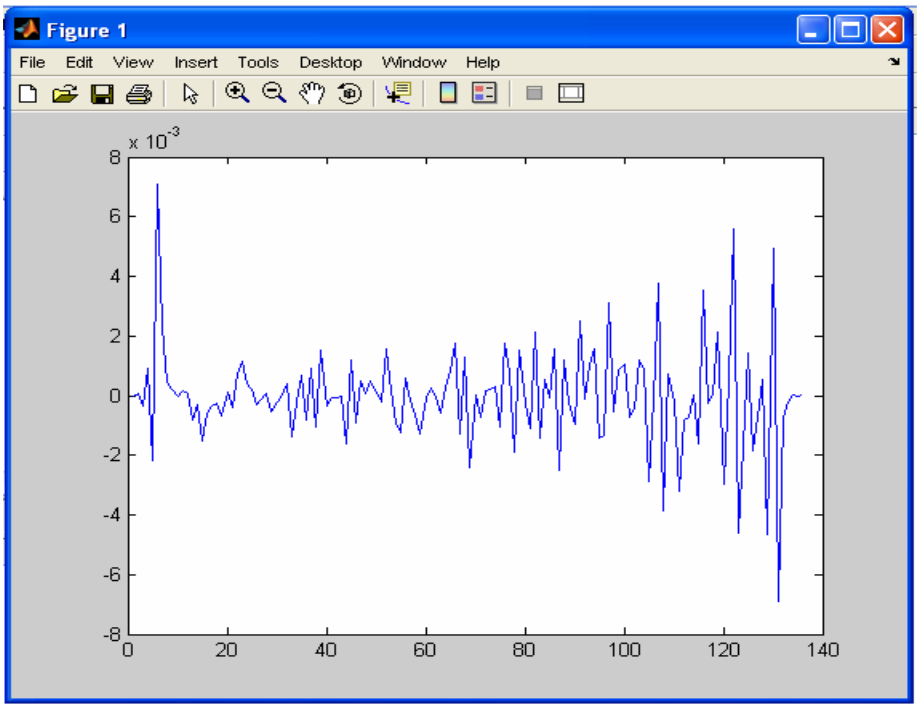


b

Figure 7. Packet(2,0) of the selected audio signal
a. Using chipscope IBA analyzer.
b. Using Mat lab software.



a



b

Figure 8. Packet (3,6) of the selected audio signal
a. Using chipscope IBA analyzer
b. Using Matlab software

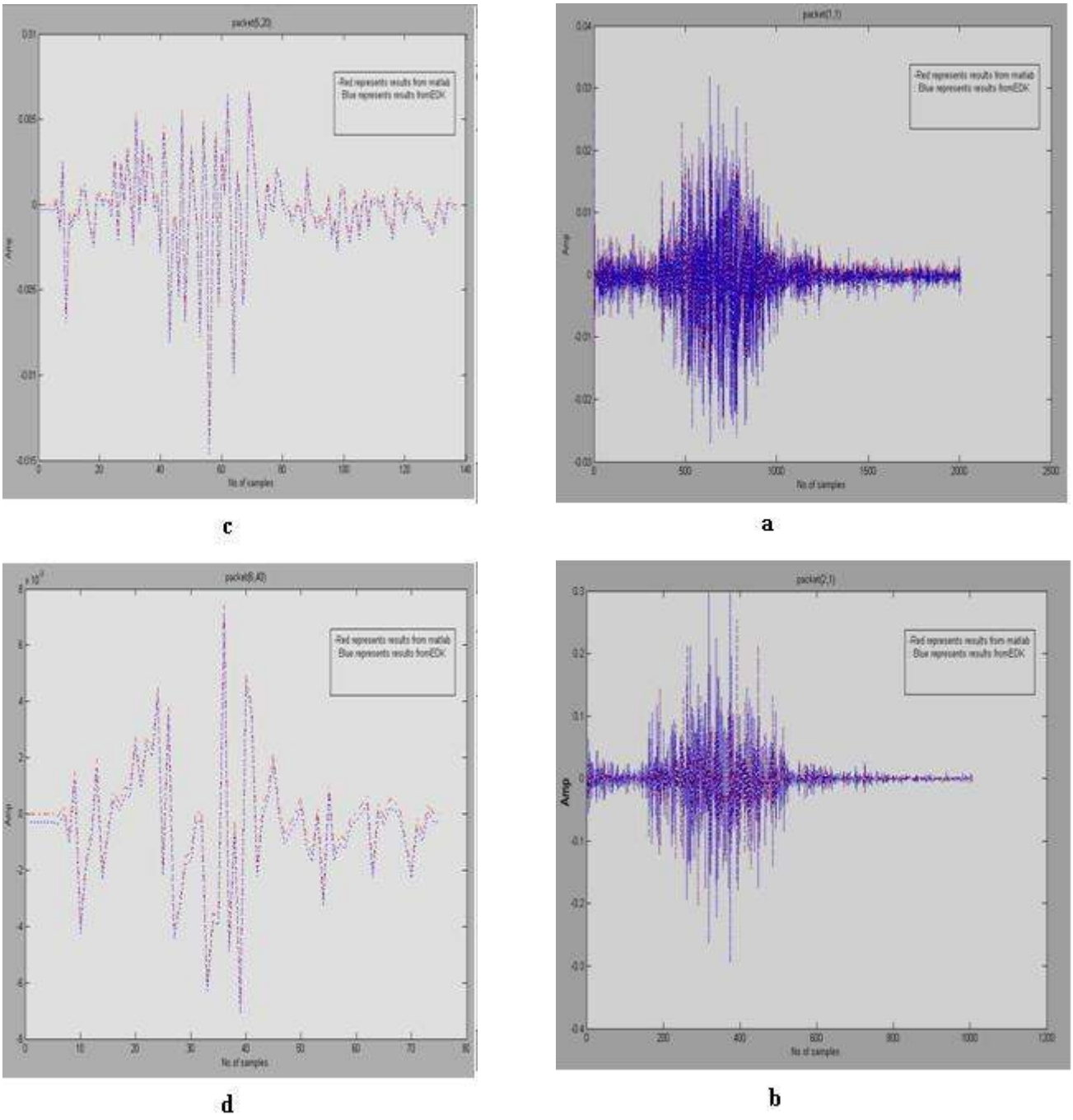


Figure 9. Selected results obtained from embedded system compared with result obtained from Mat lab. a. Packet(1,1), b. packet(2,1), c. packet(5,2), d. packet(6,40)

Conclusions :

An embedded processor system is designed and configured on Spartan 3E FPGAs slice using embedded development tools supplied by Xilinx vendor. The system is adapted to act as a wavelet packet transform tool by developing a suitable application program run on

the processor system. On the basis of the practical results the following conclusions are inferred:

- Microblaze soft core processor system with suitable peripherals can be used to obtain an efficient FPGA wavelet packet transform system.
- The designed system can decompose signals with frequency contents up to 8Mhz. This is due to the fact that the sampling rate is 16 Mega sample per second with each sample being represented by 4 bytes, resulting in 64 Mbyte data which is compliant with the capacity of the available DDR SDRAM .
- The number of decomposition levels can be set according to the user request by selecting a suitable value to the variable ndl.
- The precision of the system is improved by enabling floating point unit available in the Microblaze processor.

References :

1- CHARLES K., *An Introduction to Wavelets*, Academic Press, 1st ed, New York, 2002.

2- KILTS S., *Advanced FPGA Design*, John Wiley and Sons, 1st ed, New York, 2007.

3- BURRUS S., RAMESH A.; GUO H., *Introduction to Wavelet and Wavelet Transforms*, Prentices Hall, 1st ed, New Jersey, 1998.

4- KAYYALI A. K; SHAKER M. M; KHALIL M. R, "Design of A Wavelet Packet Decomposition System Using Field Programmable Gate Arrays (FPGAs)". *Res. J. of Aleppo Univ.* , Vol. 75, 2009.

5- AL-HAJ A., "Fast Discrete wavelet Transformation using FPGAs and Distributed Arithmetic". *International Journal of Applied Science and Engineering,* 1(2), 160-171, 2003.

6- CHEN J; HOU B, " Efficient Wavelet Transform On FPGA Using Advanced Distributed Arithmetic". *In The Proceedings Of IEEE International Conference On Electronic Measurements And Instruments (ICEMI),* PP 512- 517, 2007.

7- DUBEY R., *Introduction to Embedded System Design Using Field Programmable Gate Arrays*, Springs, Verllag London, 2009.

8- XILINX COMPANY, *Microblaze Processor Reference Guide, User Guide, UG081,* www.xilinx.com/ ISE/ Embedded/ edk_docs, 2009.

9- XILINX COMPANY*, Processor Local Bus, Datasheet, DS531*, www.xilinx.com/ ISE/ Embedded/ edk_docs, 2007.

10- XILINX COMPANY, *Multiport Memory Controller Datasheet, DS 643*, www.xilinx.com/ ISE/ Embedded/ edk_docs, 2008.

11- XILINX COMPANY, XPS Multi- Channel External Memory Controller, Datasheet, DS575, www.xilinx.com/ ISE/ Embedded/ edk_docs, 2008.

12- XILINX COMPANY, XPS UART Lite, Datasheet, DS571, www.xilinx.com/ ISE/ Embedded/ edk_docs, 2008.

13- XILINX COMPANY, *XPS General Purpose Input/ Output (GPIO),* www.xilinx.com/ ISE/ Embedded/ edk_docs, 2008.

14- XILINX COMPANY*, XPS- Timer/ Counter, Datasheet DS573*, www.xilinx.com/ ISE/ Embedded/ edk_docs, 2008.

15- XILINX COMPANY, *XPS Interrupt Controller, Datasheet, DS572,* www.xilinx.com/ ISE/ Embedded/ edk_docs, 2008.

16- XILINX COMPANY, *Local Memory Bus, Datasheet, DS 445*, www.xilinx.com / ISE/ Embedded/ edk_docs, 2007.