EFFICIENT DOWN CONVERSION TECHNIQUE BASED POLY-PHASE DECIMATION FILTER IN WIRELESS COMMUNICATION SYSTEMS [+]

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Abstract :

This paper presents a development of down conversion technique using polyphase decimation filter to work with GSM and WCDMA systems. The embedded FPGAs offer a very attractive solution that balance high flexibility, time-to-market, cost and performance. So this paper focuses on efficient design and implementation of digital down convertor for software radios on an FPGA target device. The implementation results shows an important utilization in LUPs and Slices in accordance with FPGA area and low power consumption compared with conventional design.
Key word- Down Conversion, Poly-phase filter, FPGA

تقنية المغير الخافض بالاعتماد على المختزل المتعدد الاطوار لانظمة الاتصالات اللاسلكية

بهاء علي ناصر فلاح حسن مهدي محمد عبيد براك

المستخلص

يقدم هذا البحث تطوير محول التردد باستخدام مختزل متعدد الاطوار للعمل مع منظومة الاتصالات المتنقلة و انظمة الاتصال المتعددة الشفرة من خلال الحلول المثالية التي تقدمها تقنية اف بي جي اي ذات المرونة العالية وسرعة تقديمها للمستخدم كما تؤمن كلفة قليلة. لذلك سيركز هذا البحث على تصميم مغير التردد الكفوء المبرمج للعمل مع البورد اف بي جي اي. نتائج التنفيذ تبين تامين اقل في استهلاك جداول وشرائح اقل في مساحة البورد وبذلك يكون استهلاك الطاقة اقل بالمقارنة مع التصاميم المعمول بها حاليا.
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Introduction :

The widespread use of digital representation of signals for transmission and storage has created challenges in the area of digital signal processing [1]. The applications of digital FIR filter and up/down sampling techniques are found everywhere in modem electronic products. For every electronic product, lower circuit complexity is always an important design target since it reduces the cost [2]. There are many applications where the sampling rate must be changed. Interpolators and decimators are utilized to increase or decrease the sampling rate. Up sampler and down sampler are used to change the sampling rate of digital

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signal in multi rate DSP systems. This rate conversion requirement leads to production of undesired signals associated with aliasing and imaging errors. So some kind of filter should be placed to attenuate these errors [3].

A digital down convertor (DDC) is an important part of software defined radio (SDR) based 3G or 4G baseband receivers. It shifts the spectrum of interest from its carrier frequency, i.e. intermediate frequency to baseband [4]. It also performs decimation and matched filtering to remove adjacent channels and maximize the received signal-to-noise ratio (SNR). A DDC is mainly used to down convert or decimate the GSM signal [5]. Typically lowpass filters are used to reduce the bandwidth of a signal prior to reducing the sampling rate. This is done to minimize aliasing due to the reduction in the sampling rate. Down sampler is basic sampling rate alteration device used to decrease the sampling rate by an integer factor [6]-[7]. On the receiver side, digital IF techniques can be used to sample an IF signal and perform channelization and sample rate conversion in the digital domain. Using under sampling techniques, high frequency, IF signals typically more than 100MHz can be quantified. For SDR applications, since different standards have different chip/bit rates, non-integer sample rate conversion is required to convert the number of samples to an integer multiple of the fundamental chip/bit rate of any standard. There are many advanced signal processing tasks performed in a modern digital receiver using two sub-systems called front end and back end systems. A front-end sub system operates at high-data rate and a back-end operates at low data rate or chip-rate. The front-end high-data rate FPGA DSP implements channelization functions for a multi-carrier system. Each channelizer accesses the digital IF (intermediate frequency), translates a channel to baseband and using a multi-stage multi-rate filter adjusts the sample rate to satisfy Nyquist for the selected band. The back-end processor will typically operate on multiple slower rate sample streams performing functions like rake processing, adaptive rake processing, demodulation, turbo decoding, Viterbi decoding. In a QAM system, carrier recovery, timing recovery and adaptive channel equalization will be required. Virtually all digital receivers perform channel access using a digital down-converter (DDC). A simplified block diagram of digital down convertor is shown in Figure (1). The desired channel is translated to baseband using the digital mixer comprising the multipliers M_1, M_2 and a direct digital synthesizer (DDS). The sample rate of the signal is then adjusted to match the channel bandwidth [8]-[10]. This is performed using a multi-stage multirate filter consisting of the filters $C(z)$,$G(z)$ and $H(z)$.

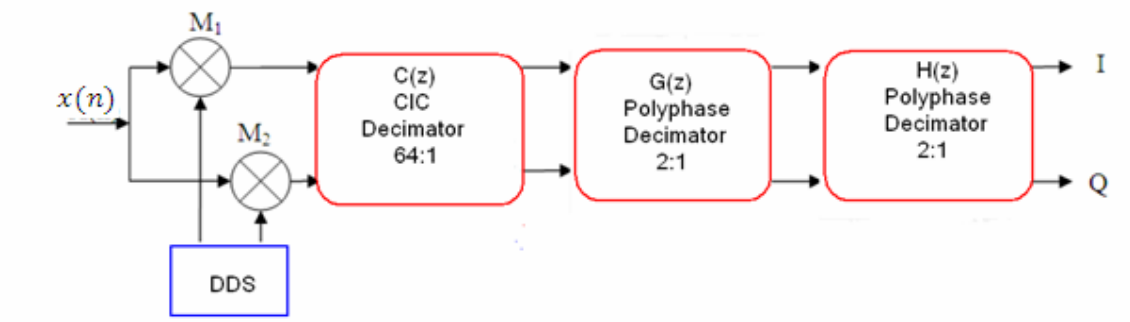


Figure1. Down conversion filter

DDC Model Based Design :

A model of Digital Down-Converter (DDC) is designed to meet the 3G and 4G specifications using a multi-section cascaded integrated comb (CIC) decimator and two Equiripple based polyphase decimators [11]-[12] with the help of Simulink and Xilinx

System Generator blocks as shown in Figure (2). The Equiripple window based technique is used which results in less number of required coefficients as compared to other window techniques to improve hardware complexity and speed. The functions performed by the developed model are complex multiplication and multi rate filtering. The proposed model consists of three major parts namely mixer section, CIC section and decimator section.

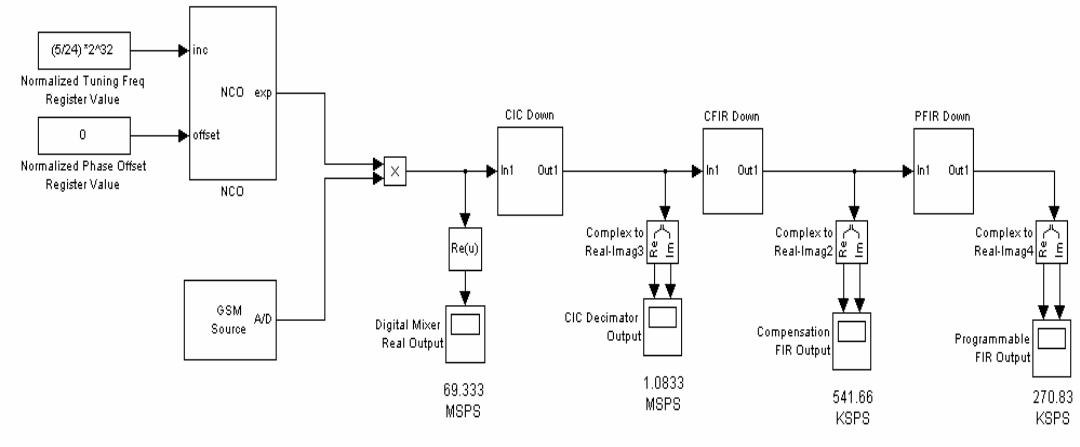


Figure2. Proposed DDC Model

1- Numerical Control Oscillator (NCO) Section

The GSM signal is generated by chirp block and filtered down from 69.333248 MHz to 270.833 KHz through the three stages of the DDC filter to recover the GSM signal**.** The DDC filter chain performs down-conversion of the input signal as well as narrow band low-pass filtering and decimation. The DDC produces low sampling rate of 270 KHz baseband signal, which signifies that the signal is ready for demodulation. The parameters of blocks in the filter chain have been modified to facilitate observation of the possibilities for modeling a customized DDC filter with SIMULINK. The GSM source block in the model is used to switch between a chirp and sinusoid signal. Accordingly, the parameters of the NCO block have been adjusted. The frequency and phase have been adjusted to 32-bit tuning frequency register value and 16-bit phase offset register value as input to the NCO block. The five-stage Cascaded integrated comb (CIC) filter with 64 decimation factors down converts the GSM intermediate frequency (IF) to lower rat as a first stage. The second stage is the adjustment of the roll-off of the CIC baseband with a 21-taps compensating Equiripple FIR filter (CFIR). Composing the closing stage of filtering and shaping of the required GSM signal using a 65-tap PFIR filter compos the final stage. Chirp signal shown in Figure 3 have a sampling rate of Fs = 69.333248 MHz and period sample of Ts = 14.4 ns, which are processed by the DDC filter according to the GSM requirements. The three stages DDC filter design and simulation are explained in following sub-section.

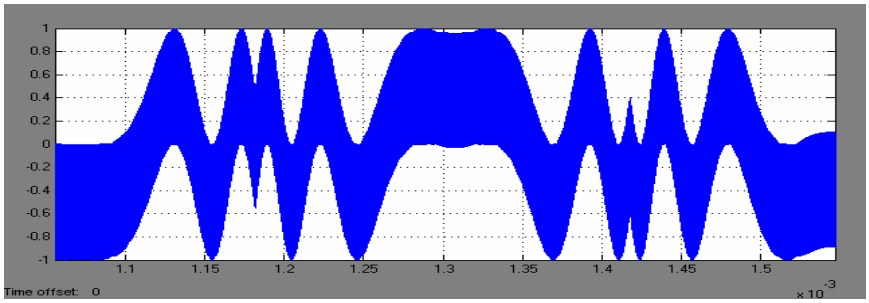
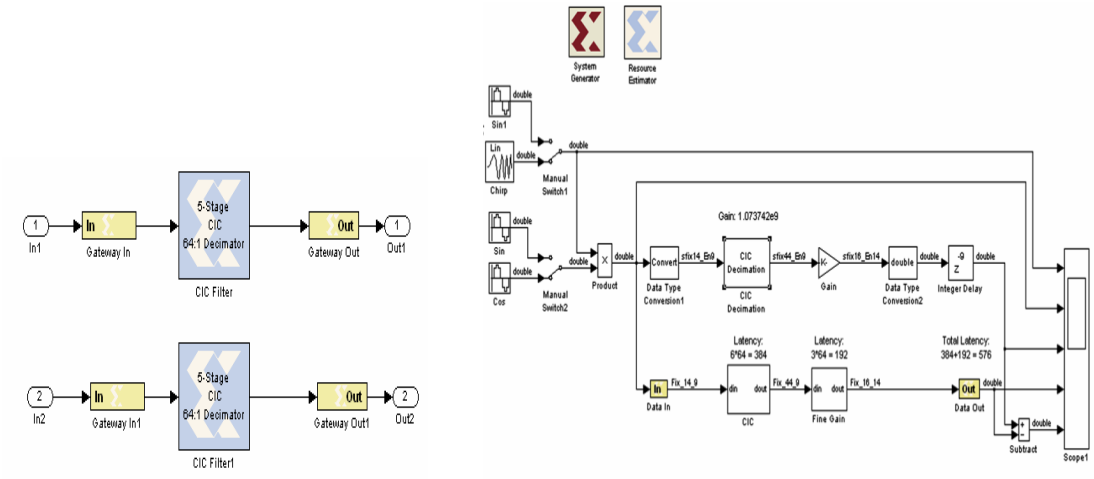


Figure 3: Chirp signal of GSM intermediate frequency (IF) 69.333 MHz

2-CIC Section

The baseband channel is highly oversampled so a simple cascade of filters, implemented as a cascaded integrator comb (CIC) [10] will be employed to initially reduce the sample rate by a factor of 64. The CIC filter $C(z)$ is multiplier less consisting only of integrator and differentiator sections. For this application a cascade of 5 integrators followed by 5 differentiators, with an embedded 48:1 rate change is used as shown in Figure (4). The initial step in CIC decimation filter implementation is to verify the MATLAB SIMULINK design in System Generator. The CIC contains five-stage integrator and differentiator, which are combined. The CIC decimator block, on the other hand, has been designed in Xilinx block.



(a) (b)

Figure4. (a) CIC Section, (b): CIC Verification

The resulting response of the CIC filters is shown in Figure (5). The mixing of chirp and sinusoidal signals in fixed point value as input of CIC1 filter and the filter responses of MATLAB design CIC2 that are synchronized by imposing delays upon the normalized CIC2 filtered signal and mixed signal at 384 + 192 = 576 are shown as well. The difference between the output of CIC1 and CIC2 is zero, which means that the design match in all stages between MATLAB design and System Generator design of the CIC filter and the verification process are satisfied with real-time constraints.

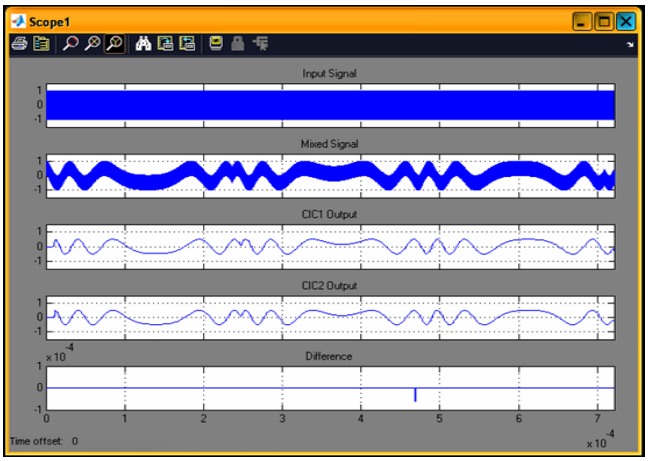
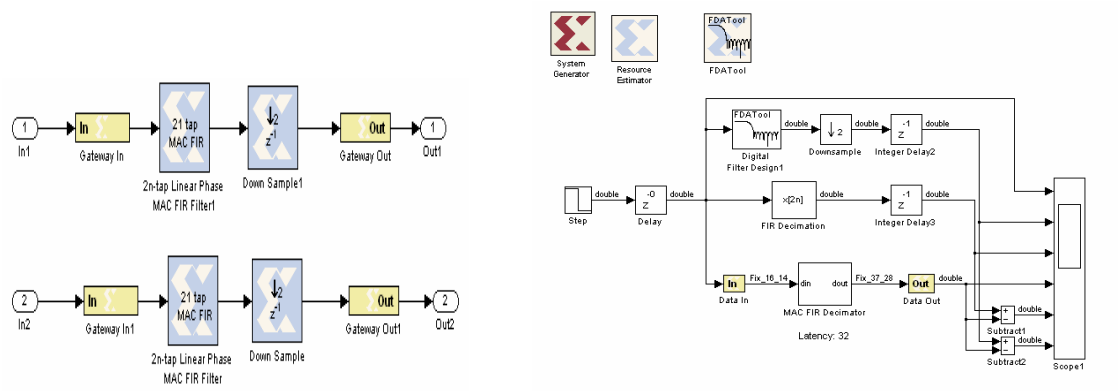


Figure 5. CIC simulation Filter Response

3-Polyphase Decimator Section

The CIC filter is followed by a cascade of two 2:1 polyphase decimators shown in Figure 6 & 8 respectively to produce the required input-to-output sample rate change of 192:1. The implementation of CFIR starts with designing the filter coefficients in fixed point values using MAC FIR decimator in System Generator as shown in Figure 6-a. Subsequently, the fixed point design of the CFIR filter is connected in parallel with the floating point design to verify the filter coefficient before implementation, as shown in Figure 6-b.



(a) (b)

Figure 6: (a): Polyphase Decimator *G*(*z*), (b): verification

The resulting response shows a slight difference between the fixed point design of the CFIR filter (MAC FIR decimator filter) and the floating point filter design in MATLAB (DF FIR decimator filter) of approximately 5×10^{-5}, as shown in Figure 7. This is mostly caused by the quantization errors resulting from the limited number of bits representing the numerical values used in the arithmetic functions such as multiplication and summation in the filtering process.

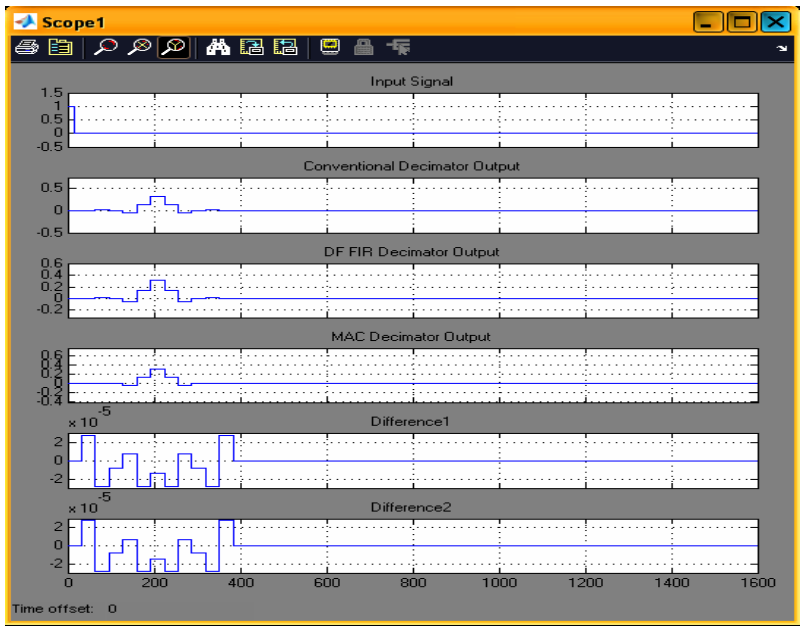
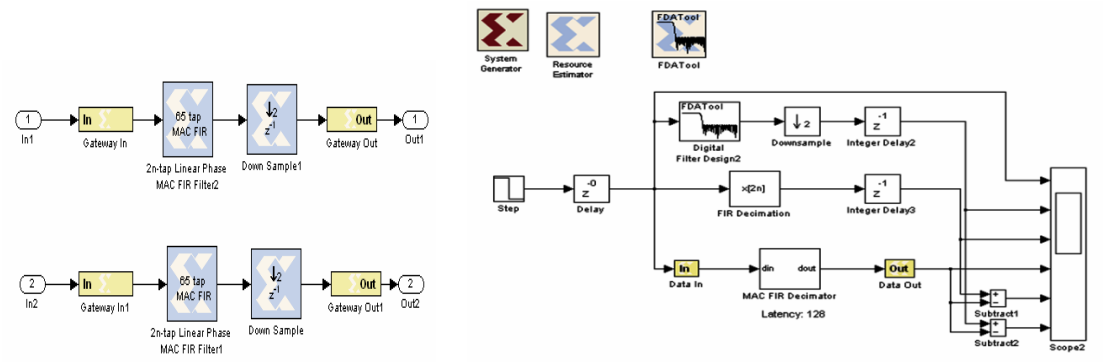


Figure 7: CFIR Filter simulation Response

A 21-tap filter is used for the polyphase decimator $G(z)$ while a 65-tap filter is employed for $H(z)$. Here 65 cycles are required to implement this filter. The PFIR filter coefficients have been designed in fixed point values using the FDATool provided by MAC FIR decimator in System Generator as shown in Figure 8-a. In Figure 8-b, the designed filter is connected in parallel with the floating point MATLAB design to verify the PFIR filter coefficients before implementation in FPGA.



(a) (b)

Figure 8: (a): Polyphase Decimator $H(z)$, (b): Verification

The resulting response of the conventional decimator and MAC FIR filter simulation in fixed point and floating point design of FIR decimator is shown in Figure 9. The resulting response of the three filters shows a slight difference of approximately 2×10^{-5}. Quantization errors resulting from the limited number of bits representing the numerical values used in the arithmetic functions such as multiplication and summation in the filtering process have caused the difference.

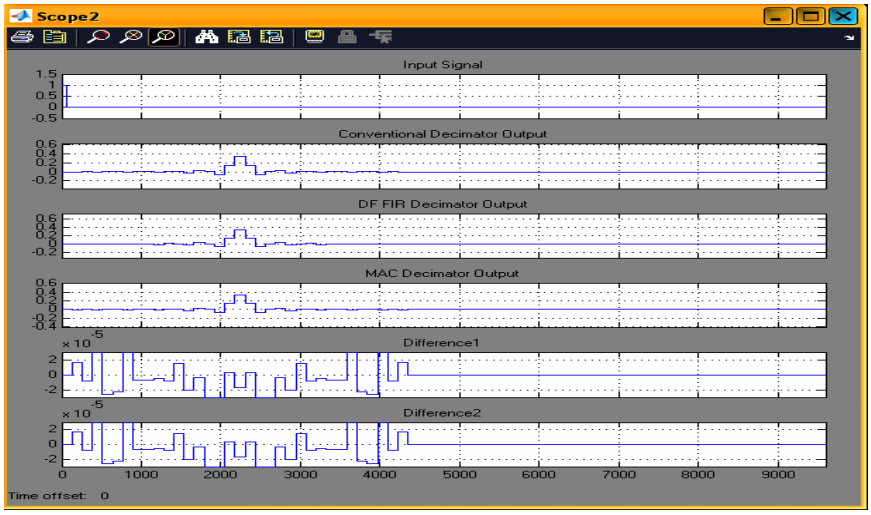


Figure 9: PFIR simulation Filter Response

According to the author [13] and the study of author [14], the complete DDC structure in fixed point values is verified with floating point values of the DDC filter as an initialization process before running the System Generator simulation in the implementation process. This establishes the correct configuration for the operation of the System Generator model, as shown in Figure (10).

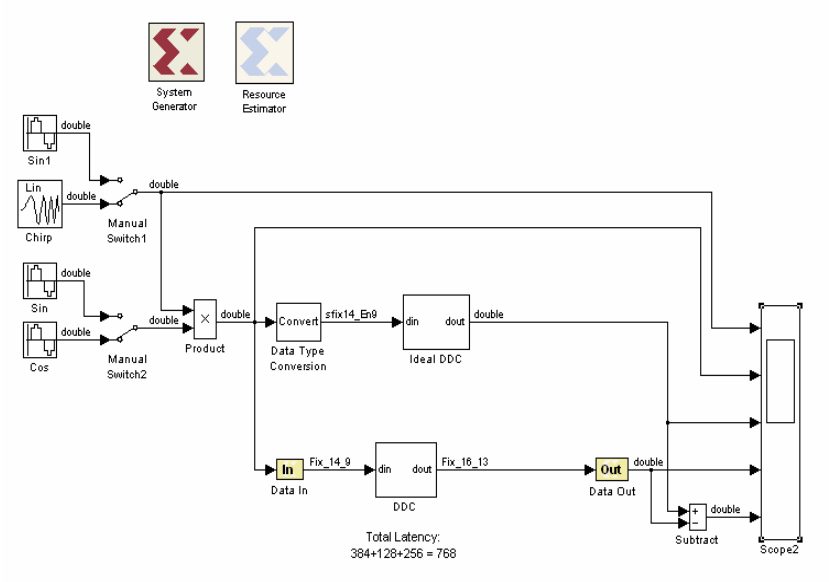


Figure 10. Verifications DDC Design

HDL Synthesis :

After the DDC filter design at fixed point has been verified with the MATLAB design in System Generator, the next step, which is the implementation of the structure in real-time form, is initiated. The complete DDC design is synthesized to create the Verilog netlist using the output options under System Generator token GUI interface and the results of the performance of map, place and route task done, by using the project navigator tool to implement the design in real time. The ISE project file is produced in the netlist directory specified in the System Generator token GUI along with the design and association with timing constraints file [15] and [16].

Verification of the DDC filter in the System Generator implementation is performed by comparing the sample outputs at various stages in the design with those produced by behavioral MATLAB model. The design is matched at all stages. Hence, the input sampling frequency of the combined filter is 69.33324 MHz. Therefore, the sampling period is set to 14.4231 ns to serve as the internal sampling of the CIC filter, and the input sampling frequency of the CFIR filter is 1.083332 MHz. As a result, the sampling period of the CFIR filter is set to 64Ts = 923.0781 ns. For the last stage, the input sampling frequency is 541.66 KHz, hence the sampling period of PFIR filter is set to 128Ts= 1846.1561 ns. The output sampling frequency of combined filter is 270.833 KHz, and thus the output sampling period is set to 256Ts = 3692.3122 ns. Consequently, the 20 ns internal sampling period for CFIR (CE_2 and CE_256) and 40 ns internal sample period for PFIR-CFIR (CE_4 and CE_128) are achieved for CFIR and PFIR respectively.

Timing characteristics comprise another important factor that affects the performance of FPGA implementation. Thus, the estimated period (required path delay) for the FPGA element must not exceed the requested clock period. For this reason, timing slack = requested period − estimated period, should have a positive value; otherwise, the integrated design has to be reworked. The estimated timing report for the synthesized design meets the time constraints, as shown in Tables 1. The constraint time represent the clock of FPGA (CLK_100) and clock enable (CE) of each stage in the DDC filter chain as illustrate in Figure 11.

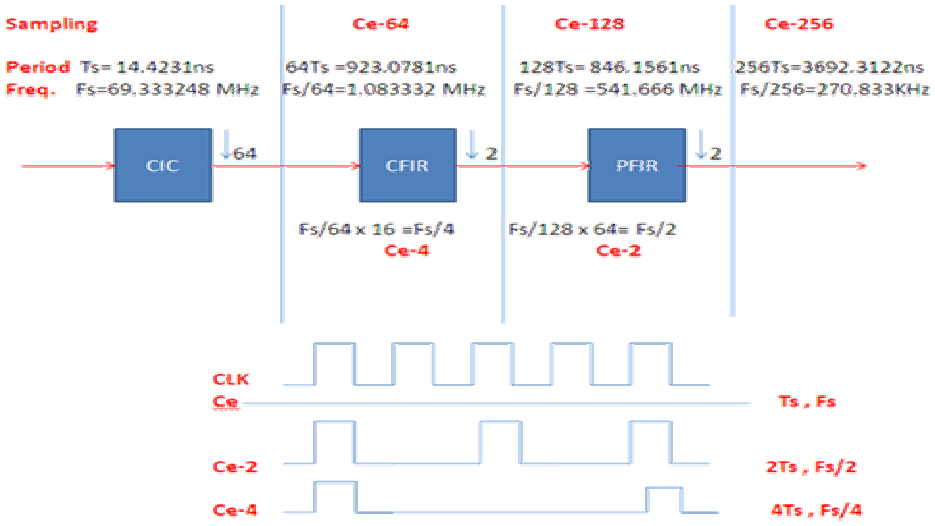


Figure 11: FPGA Timing constraint of DDC filter

In order to ensure that no timing violation (like period, setup or hold violation) will occur in the working design, timing constraints must be specified. Basic timing constraints that should be defined include frequency (period) specification and setup/hold times for input and output pads. The first is done with the PERIOD constraint, the second - with the OFFSET constraint. Timing constraints for the FPGA project are defined in the UCF file [15].

Table 1: DDC Place And Route Timing Report

Constraint	Check	Worst Case Slack	Best Case Achievable	Timing Errors	Timing Score
TS_clk_b81e7c3a = PERIOD TIMEGRP "clk_b81e7c3a" 10 ns HIGH 50%	SETUP	3.981ns	6.019ns	0	0
	HOLD	0.502ns		0	0
TS_ce_2_b81e7c3a_group_to_ce_2_b81e7c3a_group = MAXDELAY FROM TIMEGRP "ce_2_b81e7c3a_group" TO TIMEGRP "ce_2_b81e7c3a_group" 20 ns	SETUP	12.101ns	7.899ns	0	0
TS_ce_2_b81e7c3a_group_to_ce_256_b81e7c3a_group = MAXDELAY FROM TIMEGRP "ce_2_b81e7c3a_group" TO TIMEGRP "ce_256_b81e7c3a_group" 20 ns	SETUP	17.645ns	2.355ns	0	0
TS_ce_128_b81e7c3a_group_to_ce_2_b81e7c3a_group = MAXDELAY FROM TIMEGRP "ce_128_b81e7c3a_group" TO TIMEGRP "ce_2_b81e7c3a_group" 20 ns	SETUP	18.051ns	1.949ns	0	0
TS_ce_4_b81e7c3a_group_to_ce_4_b81e7c3a_group = MAXDELAY FROM TIMEGRP "ce_4_b81e7c3a_group" TO TIMEGRP "ce_4_b81e7c3a_group" 40 ns	SETUP	34.058ns	5.942ns	0	0
TS_ce_4_b81e7c3a_group_to_ce_128_b81e7c3a_group = MAXDELAY FROM TIMEGRP "ce_4_b81e7c3a_group" TO TIMEGRP "ce_128_b81e7c3a_group" 40 ns	SETUP	38.279ns	1.721ns	0	0

The optimization of timing performance for real-time process reports show zero timing error and the internal sampling period between each DDC stage implementation is satisfied. The worst case slack is the difference between constraint clock and best case achievable and should be positive (i.e. the best case achievable must not exceed the constraint clock), for example: if the constraint clock period = 20 ns and the best case achievable = 7.899 ns, then the worst case slack = 20 −7.899= 12.101 ns. Due to the positive value of worst case slacks the ISE software produce zero timing error and zero timing score for each DDC filter stage. Because of the absence of error and warning for design rule checker (DRC), the configuration of the DDC filter has been successfully implemented in FPGA using the ISE software through the translate, map, place, and route steps. The project status of ISE software generates the DDC utilizing summary as shown in Table 2. The table lists the total number of slices and look-up tables (LUTs) used in this design. In each slice they are two LUTs and two FFs, during the PAR, the ISE software put all necessary LUTs close to each other for minimum propagation of data, for that some LUT inside slice not used and in some slice only FFs is used without LUT so, the number of LUTs cannot be calculated manually, therefore the LUTs could be less or more than Slices depend on software optimization. The device utilization summary generated by ISE software represents the available logic elements in FPGA and logic elements used by the in hand project been designed. The percentage of used logic elements to the available logic elements is calculated as follow:

$$\text{Utilization \%} = \frac{\text{used logic elements}}{\text{available logic elements}} X\ 100$$, for examples:

Utilized number of Slice Flip Flop = (946/30720) x 100 = 3%
Utilized number 4-input LUTs = (530/30720) x 100 = 1%
Utilized number of occupied Slices = (661/15360) x 100 = 4%
Utilized number of bonded IOBs = (31/448) x 100 = 6%

Table 2: DDC project status and device utilization summary

DDC_CW Project Status			
Project File:	ddc_cw.ise	**Current State:**	Placed and Routed
Module Name:	ddc_cw	• **Errors:**	No Errors
Target Device:	xc4vsx35-10ff668	• **Warnings:**	911 Warnings
Product Version:	ISE 9.2i	• **Updated:**	Wed Mar 2 13:14:22 2011

DDC_CW Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	946	30,720	3%	
Number of 4 input LUTs	530	30,720	1%	
Logic Distribution				
Number of occupied Slices	661	15,360	4%	
Number of Slices containing only related logic	661	661	100%	
Number of Slices containing unrelated logic	0	661	0%	
Total Number of 4 input LUTs	755	30,720	2%	
Number used as logic	530			
Number used as a route-thru	7			
Number used as Shift registers	218			
Number of bonded IOBs	31	448	6%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Number used as BUFGCTRLs	0			
Number of FIFO16/RAMB16s	2	192	1%	
Number used as FIFO16s	0			
Number used as RAMB16s	2			
Number of DSP48s	2	192	1%	
Total equivalent gate count for design	158,984			
Additional JTAG gate count for IOBs	1,488			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Depending on the number of FPGA logic resources used in the DDC filter, the ISE software calculates the power consumption of the DDC filter using the X-Power Analyzer tool and generates the details of voltage (V), current (mA), and power (mW), which will be dissipated in the implementation process, as shown in Table 3. The power consumed in the proposed design identified by the X-Power Analyzer tool is 83.01 mW in the dynamic power consumption and 191.71 mW in the quiescent power consumption.

Table 3: Power consumption report after DDC implementation

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.2		
Dynamic		69.17	83.01
Quiescent		159.76	191.71
Vccaux	2.5		
Dynamic		0.00	0.00
Quiescent		162.50	406.25
Vcco25	2.5		
Dynamic		0.00	0.00
Quiescent		0.00	0.00
Total Power			680.97
Startup Current (mA)		0.00	
Battery Capacity (mA Hours)			0.00
Battery Life (Hours)			0.00

Summary | Power Subtotals | Current Subtotals | Thermal

Figure (12) shows the overall magnitude response of the proposed DDC filter and conventional DDC filter, which is produced by author [17] respectively. In proposed DDC filter the first adjacent band rejection starts with -45 dB, whereas in the conventional DDC filter, the first adjacent band rejection starts with -25 dB. Furthermore, the proposed filter provides -117 dB in the blocker band response, whereas the conventional filter provides only -105 dB.

These improvements have been achieved because of the different weights used in the different band. Additionally, the weights at the pass-band region are set to 30 times more than the stop-band weights to improve the adjacent band rejection and blocker response. Consequently, the improvement achieved in the adjacent band rejection is 18% and 11% in blocker requirements more than that of the conventional filter.

Figure (13) represents the overall pass band response after zoom-in of proposal DDC filter and conventional filter produced by [17]. As seen from the two graphs, the pass-band ripple of the proposed filter in the required band (0–80 KHz) is less than that of the conventional filter in the same graph scale. The peak to peak ripple is 0.012 dB in the proposal filter while 0.03dB in conventional DDC filter.

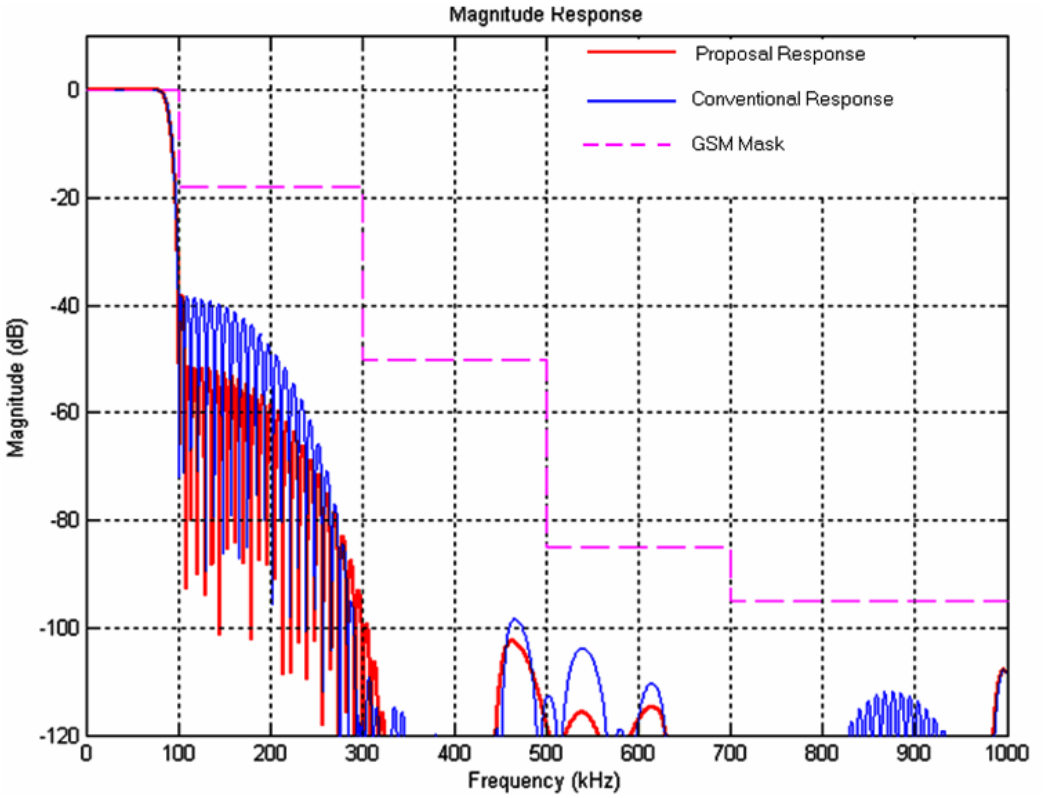


Figure 12: Overall DDC responses of proposal and conventional filter

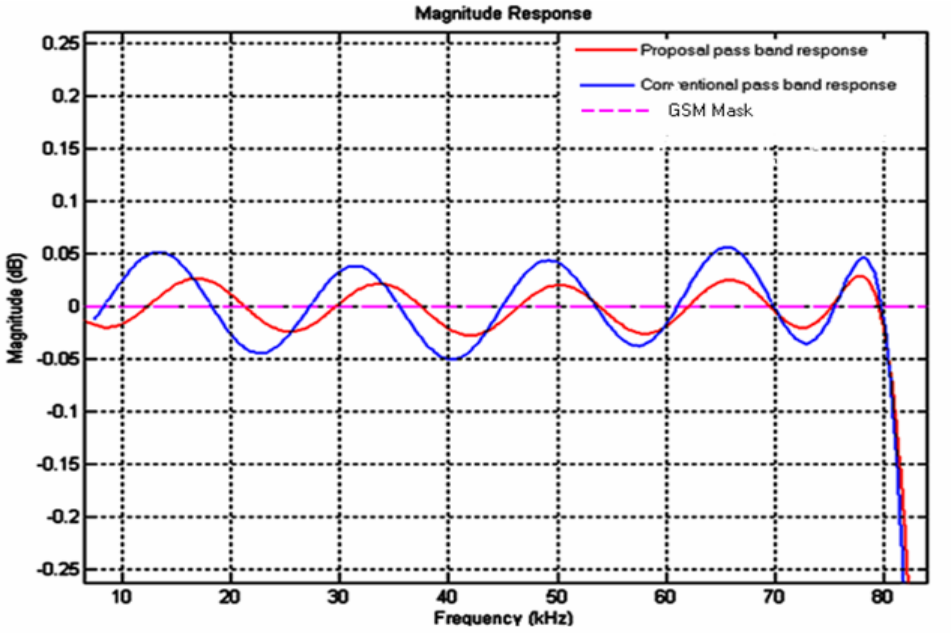


Figure 13: Overall Pass-band response of proposed and conventional DDC filter

After zooming-in more the pass-band response of the proposed filter, the pass-band ripple is found to be (0.012 dB pp), as shown in Figure 13. The resulting pass-band response shows an important development in the pass-band ripple by 40%, which is significantly lower compared with the conventional filter. Thus, the result shows that the development of the pass-band ripples have been achieved using the proposed algorithm.

The transition width of the CFIR filter is changed from 20 to 10 kHz to increase the filter order, which results in the reduction of the maximum absolute error. This change does not affect the overall transition width of the combined three filters in the DDC design. Therefore, the resulting transition width of the combined filter remains at 20 kHz. The resulting transition width of the GSM system for the proposed filter response is highlighted in Figure (12) and could be calculated from Figure (14). The normalized pass-band frequency is 2.3 π rad/sample, and the normalized stop-band frequency is 2.88 π rad/sample. Therefore, the transition width can be calculated as:

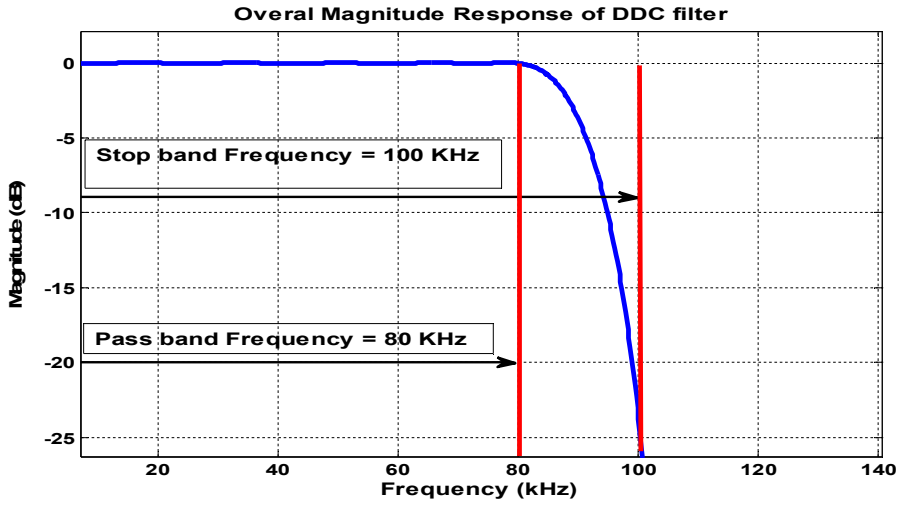


Figure 14: Pass-band response – GSM mode with transition width of 20 kHz

Table 4 shows the filter specification comparison of the results obtained with the conventional design in terms of the pass-band ripple, adjacent band rejection, and blocker requirements of the filter. The proposed DDC filter decrease the pass band ripple by 40% less than the conventional filter and this development could enhance the capability of the filter to avoid any distortion and error in the desired signal and decrease the power consumption.

Table 4 DDC filter specifications comparison

PARAMETERS	Conventional GSM MODE			PROPOSED DDC Filter (2011)	Improvements
	Naina R. (2007)	Douglas L. (2008)	Texas Instruments (2009)		
Pass-band Ripple	−0.05dB	−0.1dB	−0.03dB	− 0.02 dB	20%
Adjacent-band rejection	−125dB	−20dB	−25 dB	− 45dB	18%
Blocker Requirements	−110dB	−85dB	−105dB	− 117dB	11%

The proposed filter provides less power consumption 20% less than the conventional filter. In the adjacent band rejection, the proposed filter provides more attenuation to overcome the interference that may happen in the channel by 18% more than the conventional filter. The attenuation of the blocker requirements in the filter response was increased by 11% more than the conventional filter; therefore, the improvement in the filter capability to avoid and prevent any effect of spectral replicas from the following stages has achieved.

Conclusions :

In this paper, an optimized polyphase design using System Generator is presented to implement GSM based digital down convertor for software defined radios. Equiripple based polyphase decomposition technique is used to optimize the proposed DDC design in terms of speed and area. The proposed design can operate at maximum frequency of 160 MHz by consuming power of 83.01 mW at 25 °C junction temperature. The proposed model is consuming very less resources on Virtex-4 based target device to provide cost effective solution for SDR (3G & 4G) wireless communication applications. The implementation results shows an important utilization in LUPs and Slices in accordance with FPGA area and low power consumption compared with conventional design. This work will gave better performance with some tunning in filter.

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