DESIGN AND SIMULATION OF THE DIGITAL UP CONVERTER (DUC) FOR GSM SYSTEM USING MATLAB AND SYSTEM GENERATOR [+]

Maher Ibraheem Gama [*]

Abstract :

This paper presents the design and simulation of the Digital Up Converter (DUC) in system generator. DUC is a digital circuit which generating digital Intermediate Frequency (IF) signal from low complex digital baseband signal. The DUC provides pulse shaping, interpolation and frequency translation where the up-sampled signal is shifted from centered frequency (2.166 MHz) to intermediate frequency. Due to Wideband Global System Mobile (GSM) specifications, the DUC is to pulse shaped and up sampled the baseband signal by a factor of 16. The DUC up sampled the signal up to 69.333MHz.

Keywords: DUC; Intermediate Frequency (IF); GSM

تصميم ومحاكاة المغير الرافع الرقمي لمنظومة جي اس ام باستخدام برنامج ماتلاب ومولد النظام

ماهر إبراهيم جمعة

المستخلص :

يقدم هذا البحث تصميم ومحاكاة مغير التردد الرقمي المبرمج باستخدام برنامج ماتلاب و مولد النظام. هذا المرشح الرقمي يولد التردد المتوسط من اشارة المعلومات الاصلية ذات التردد الواطيء. كما يحقق تشكيل نبضة وتحويل التردد النظام لمنظومة جي اس ام بمقدار 16 لتصبح ضمن حزمة التردد المتوسط البالغة 69.333 ميكا هيرتز.

1. Introduction :

One of the Xilinx System Generator advantages is its ability to use FDATool in the loop with Simulink simulations. The input was fed from computer and the output was looped back to computer. This special block's ports haves names and types that are similar to the original design ports. DUC design is simulated on Xilinx block set which provides a useful board for designing and verifying design into actual application. It is a multipurpose board can be used for many designs such as software defined radio and wireless communication system implementation [1]

[+] Received on 15/7/2012 , Accepted on 26/1/2014

[*] Assistant Lecturer / Institute of Technology / Baghdad

2. DUC Design and Simulation :

The FPGA is popular for prototyping integrated circuit and embedded system. Configuration of FPGA is done by specifying how the chip works with a logic circuit or a source code using a hardware description language (HDL) [2].
Implementing DUC in FPGA is not an easy task as many parameters need to be included. One of the Xilinx System Generator advantages is its ability to use FPGA hardware in the loop with Simulink simulations. For this design, System Generator is used in order to run the design which has been programmed into the Xilinx board. Many facilities is provided by System Generator tools; control the design hardware during the Simulink's simulation which it interconnected with the design in computer. The design and FPGA board are connected using JTAG cable. The input was fed from computer and the output was looped back to computer. An effective way to verify the design in the real hardware is by use the system generator DSP block set to creates a special co-simulation block that will run in parallel with the FPGA board. This special block's ports haves names and types that are similar to the original design ports.
As known, the chip rate for GSM is 2.166 MHz. Thus the IF sampling rate must be higher than the chip rate. The design will be up sampled by 16 which means that the IF rate is 69.333MHz. The system clock of Xilinx block set need to be included so that the result will behave as it should be. The system clock needs to be a multiple of the IF sample rate and preferably a multiple of six. In DUC, pulse shaping, interpolation and frequency translation are the processes that executed in the design. Transmit spectral mask in the design must be met in order to fulfill the GSM requirement. The requirements are obtained from Texas Instruments [3]. Table 1 shows the GSM requirements in IF band.

Table (1): GSM requirements in IF band

Clock rate	2.166 MHz
Pass-band width	80kHz
DUC output rate	69.333MHz

As mentioned above, the design of DUC needs to match GSM requirements. In DUC, filtering the most important part to design and it has to be designed thoroughly according to required spectral mask. A good method is to separate the rate conversion into multiple interpolation stages rather than upsample the rate in single stage. Root Raised Cosine (RRC) is a favorable filter to do pulse shaping as it transition band is shaped like a cosine curve and the response meets the Nyquist Criteria. After filtering, the signal needs to up sample to remove aliasing effects in this process. One way to design the configuration of the interpolation filter is using MATLAB tools; Filter Design and Analysis Tool (FDA Tool). FDA Tool is a graphical user interface (GUI) that provides designer to set filter specifications as required before design the filter into Xilinx System Generator. Figure 1 shows the RRC filter design for DUC.

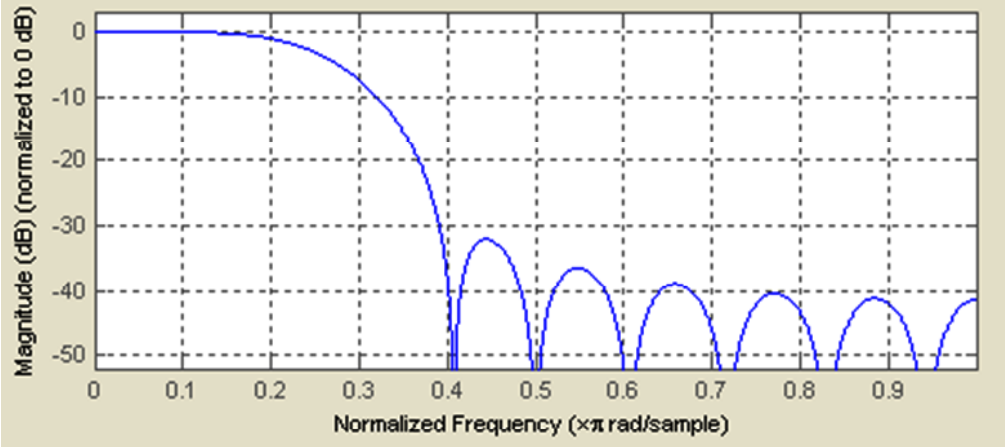

Figure (1): RRC Filter Design for DUC.

As we can see from Figure (1), the signal is pulse shaped within the spectral mask range. Thus, the RRC filter design was met GSM requirements. Then, the interpolation filter was set up according to GSM requirements. In RRC channel, the signal is up sampled by a factor of 2. Due to this, the signal needs to up convert to 2 as the IF is 69.333MHz. It is impractical to up convert the signal simultaneously. The rate conversion was divided into three cascaded filter chain which each filter was up sampled by 2. The filter used is LPF filter as it reduced hardware complexity hence has less computational power [4]. Figure (2) shows the block diagram of GSM interpolation filter.

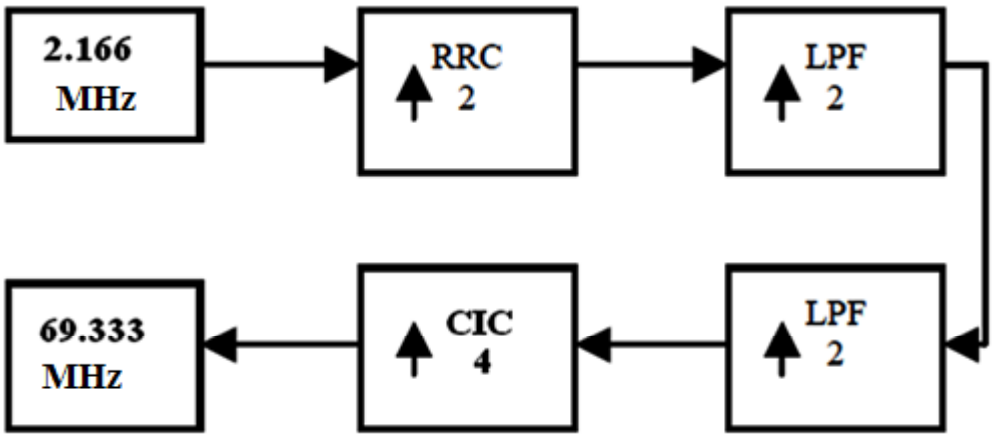

Figure (2): Block Diagram of GSM Interpolation Filter

The first RRC filter sample rate is:

$$F1 = 2.166 \times 2 = 4.33 \text{ MHz} \quad (1)$$

By using MATLAB FDA Tool, the first LPF was designed which consists of 65-tap Equiripple PFIR filter. Figure (3) shows the magnitude response of first LPF interpolator filter. It can be seen that the stop band attenuation is around 200dB.

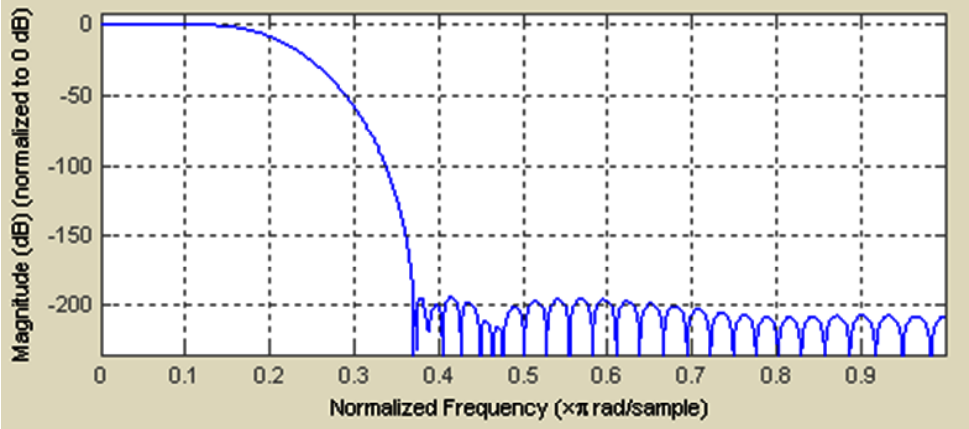

Figure (3): Magnitude Response of First LPF Interpolator Filter.

The second LPF interpolator filter is
:

F2 = 4.33 x 2 = 8.66 MHz (2)

A 21-tap equiripple LPF interpolator was designed for second LPF interpolator filter to meet the specifications and the simulation result is shown in Figure 4. With the filter coefficient quantized to 16 bits, the stop band attenuation is 100 dB.

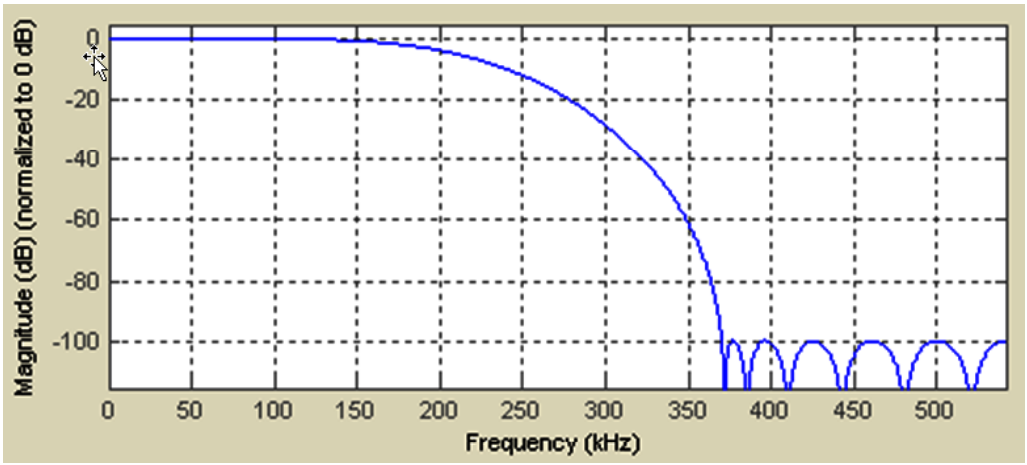

Figure (4): Magnitude Response of Second LPF Interpolator Filter.

For the third stage LPF interpolator filter sample rate is:

F3 = 8.66 x 2 = 17.328 MHz (3)

Finally, the signal was up sampled in the last CIC filter in which it produced higher IF sampling rate from the original signal sample rate using 5-stages CIC interpolated filter with 4 interpolation factor.

F4= 17.328 x 4 = 69.333 MHz

Up to this stage, pulse shaping and interpolation filter were succeeded before future implementation in Xilinx System Generator. All the filter designs above were met the required specifications of GSM.
After pulse shaping and interpolating single carrier baseband signal to higher sampling rate, the signal needs to be shifted from 0Hz to intermediate frequency in the range of [-Fs/2, Fs/2],where Fs =69.333MHz. This process is called frequency translation. Frequency translation required Direct Digital Synthesizer (DDS) and a mixer. A mixer consists of complex multiplier which multiplies upsampled signals with complex exponential that were generated through DDS. DDS was built by quadrature synthesizers for constructing digital down and up converters, demodulators and implementing various types of modulation scheme [5] [6].

3. DUC Simulation Results :

After completing synthesizing and simulating the filter parameter in MATLAB FDA Tool, the DUC design was redesign in Xilinx System Generator using the parameters simulated in FDA Tool. The parameters have been verified before and it is easy for designer to implement in the System Generator environment. The block diagram of GSM DUC is shown in Figure 5.

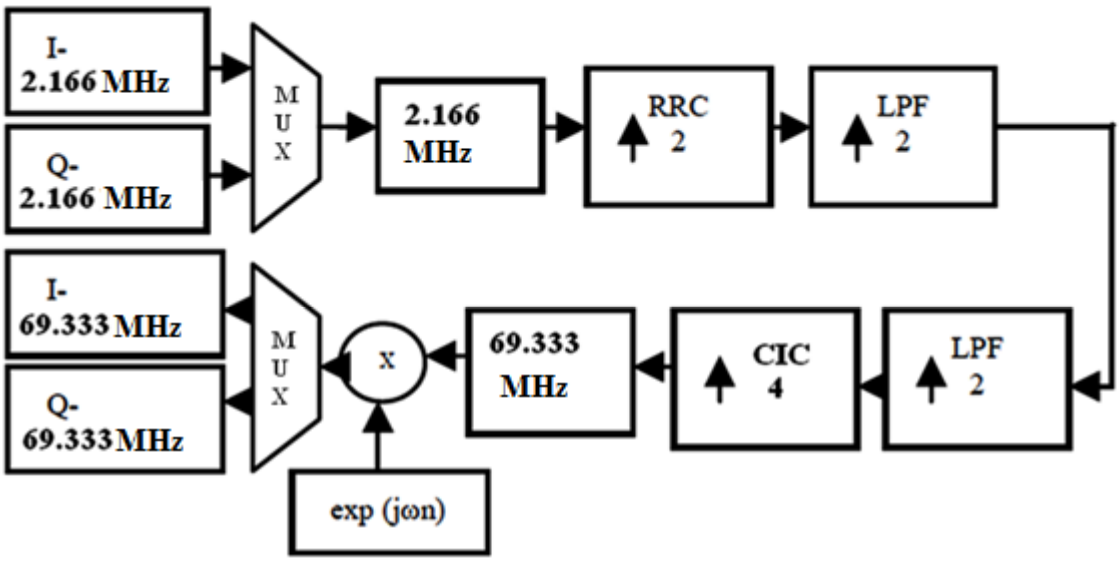

Figure (5): GSM DUC Block Diagram.

The top level DUC implementation using System Generator is displayed in Figure 6 which it consist of two subsystems that were Interpolation Filters subsystem and Mixer Subsystem.

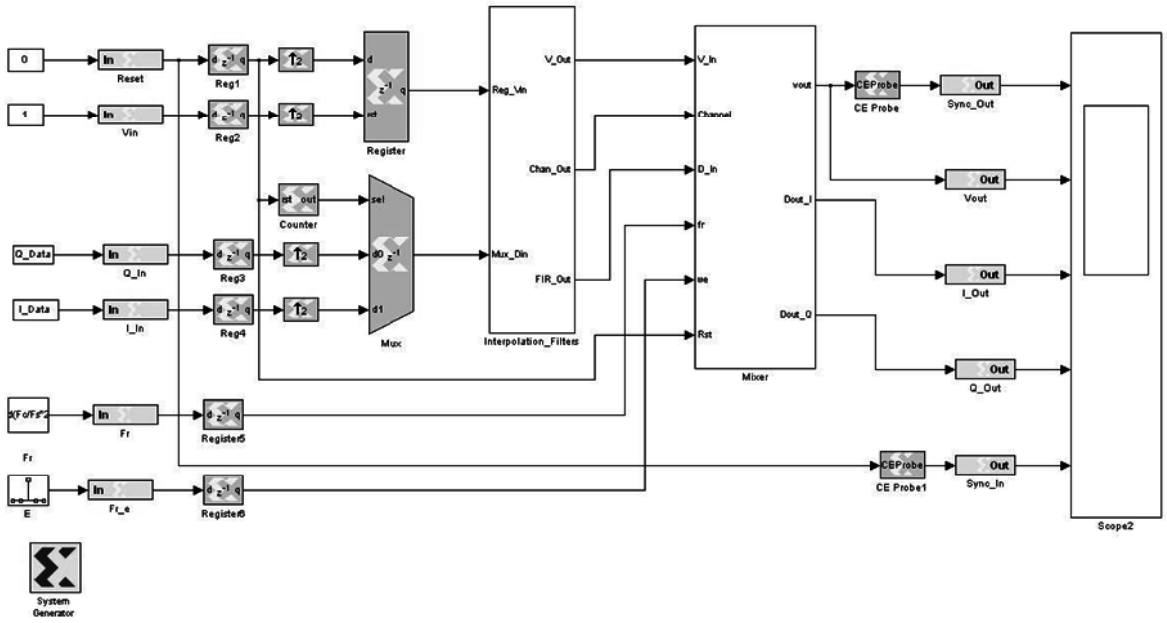

Figure (6): DUC Implementation Using System Generator.

Figure 7 shows the DUC interpolation filter subsystem where the parameters have been verified and are set according to MATLAB FDA Tool design simulation and Figure 8 shows the subsystem of the mixer respectively.

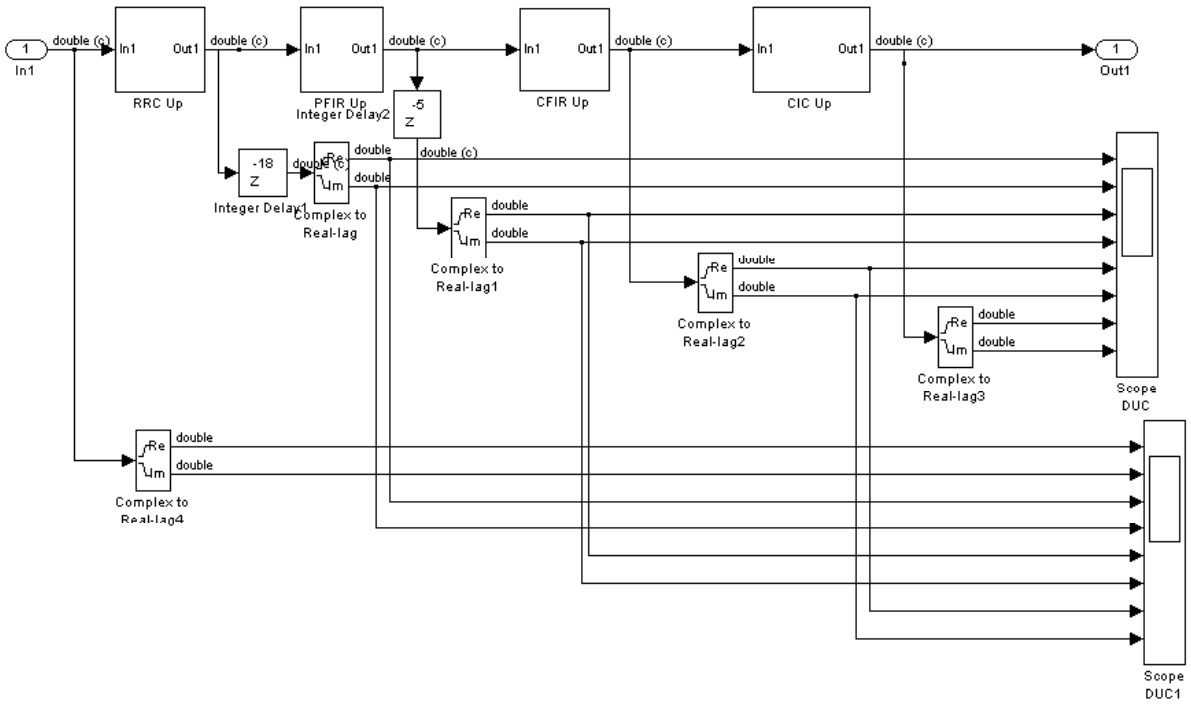

Figure (7): Interpolation Filter Subsystem.

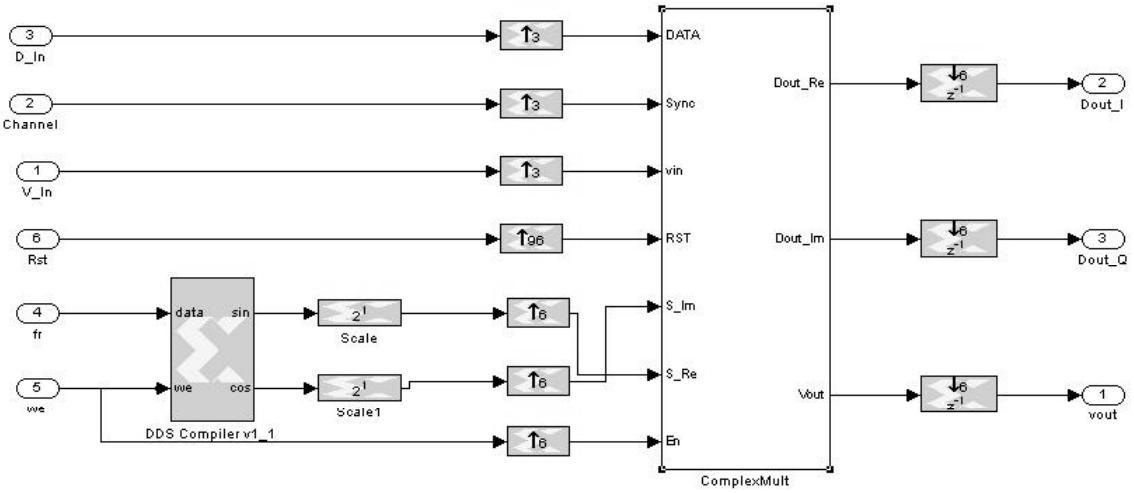

Figure (8): Mixer Subsystem.

The simulation results of DUC interpolation filter shows the 4 stages filtering process. The QAM signal is shaped first by RRC filter and up-sampled from 2.166 MHz to 69.333MHz by two stages FIR filters that are PFIR and CFIR. Finally the GSM signal is up sampled by the CIC interpolator as illustrated in Figure 9. One can see the two channels (I/Q) of the GSM signal were up-sampled successfully using DSP system generator block set after verifying the floating point values in MATLAB with fixed point values for real time purpose before implementation.

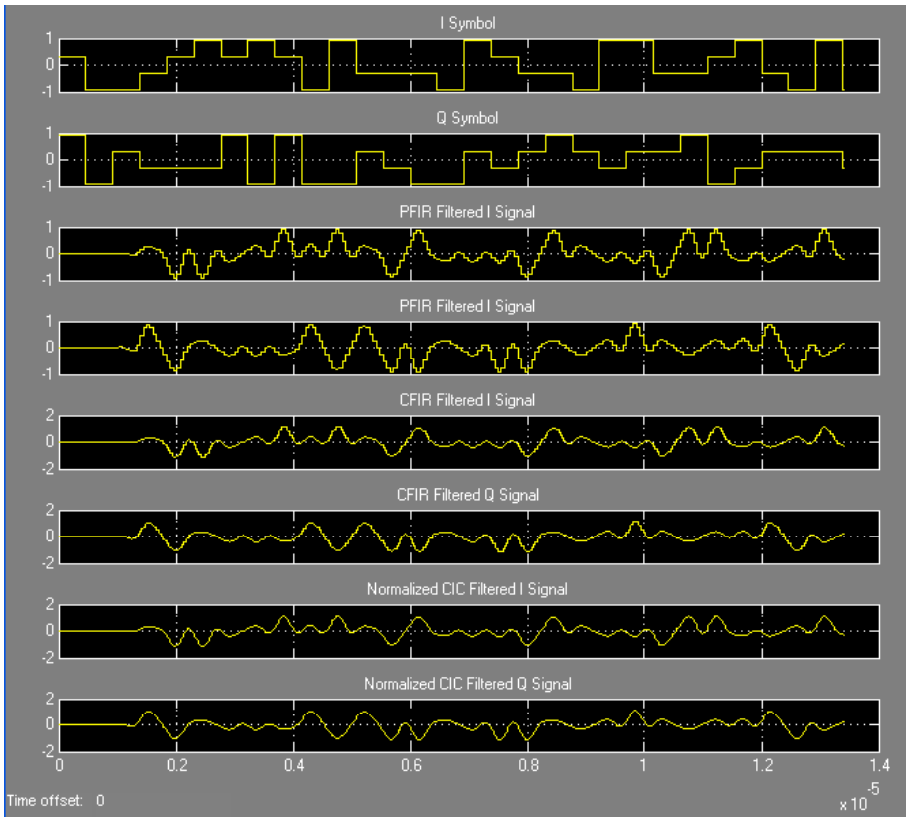

Figure (9): The GSM signal with three stages up-sampling

4. DUC Implementation Design Flow :

To implement the DUC model in FPGA, Xilinx offers numerous tools to download the designed model as a bit-stream to FPGA [7]. Figure 10 shows the simulation and implementation steps by using the MATLAB and Xilinx System Generator's blocks. The ModelSim blocks are an assistant block used to design the Verilog module of integrated design. The ModelSim output is fed back to SIMULINK for verification.

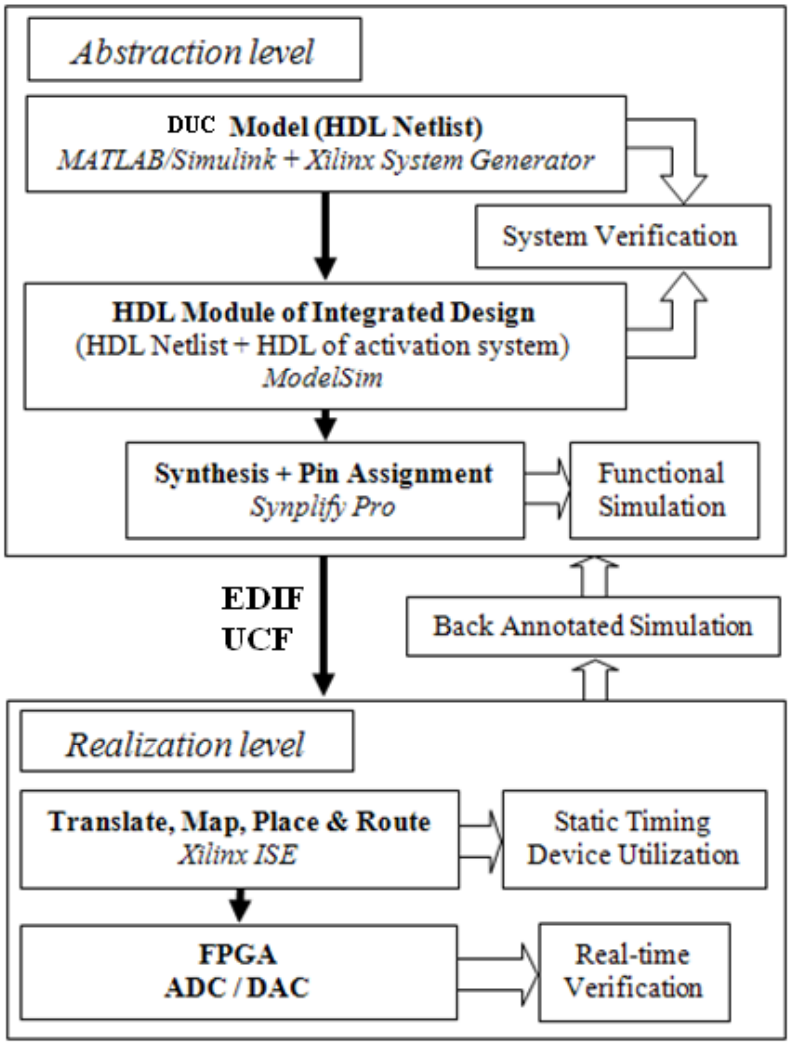

Figure (10): Xilinx System Generator based design flow

The implementation steps shown in Figure 11 are read in the constraints file that consists of three major steps: translate, map, and place and route. The translate step essentially flattens the output of the synthesis tool into a large single netlist. A netlist in general, is a large list of gates which is compressed at this stage to remove any hierarchy. The map step groups the logical symbols in the flattened netlist into physical components, specific to the target device. The place and route step places each of these physical components onto the FPGA chip and connects them through the switch matrix and dedicated routing lines.

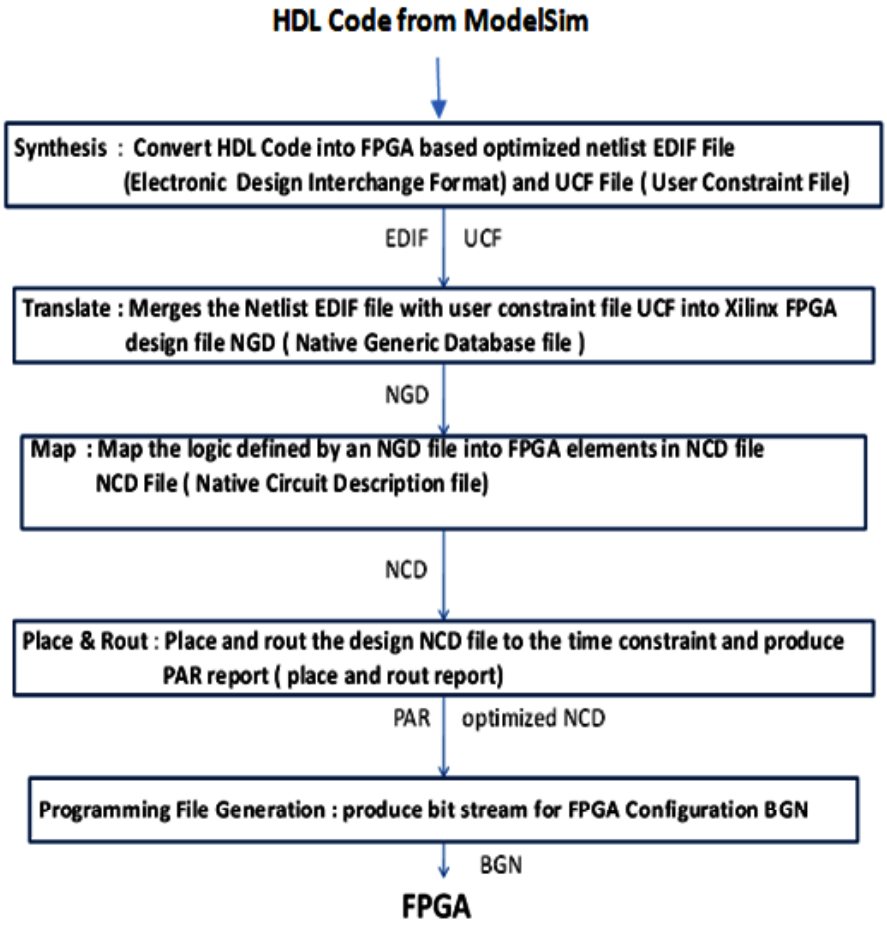

Figure (11): FPGA Implementation steps

4.1 HDL Design :

The ModelSim software is used to design HDL module activation of plug-in Avnet Electronic Marketing P240 Analog Module and Virtex-4 FPGA on-board ICS8442 Programmable low voltage differential signaling (LVDS) Clock Synthesizer with exact configurations. The HDL module of activation system should include all the specifications, characteristics, and features described above to ensure that ADC and DAC in P240 can function correctly. The HDL module of activation system and HDL netlist of DUC system in Verilog language are verified first before they are combined to become the HDL module of the integrated design. The simulated result of HDL netlist of the DUC system is similar to the simulation result of the System Generator design.

4.2 Synthesis of Integrated Design :

Although Xilinx ISE has its own synthesis tool called XST (Xilinx Synthesis Technology), it can only synthesize HDL netlist generated from the System Generator. Therefore, the Synplify Pro software is used to perform logic synthesis for the HDL module of integrated design in two stages.

1. Logic compilation and optimization: Compile the Verilog HDL module of integrated design to Xilinx FPGA structural elements and then optimize the integrated design to make it as small as possible to improve circuit performance.
2. Technology mapping: Map the optimized integrated design to Xilinx FPGA logic components using architectural-specific technique.

Timing characteristics comprise another important factor that affects the performance of FPGA implementation. Thus, the estimated period (required path delay) for the FPGA element must not exceed the requested clock period. For this reason, the timing slack (requested period - estimated period) should have a positive value; otherwise, the integrated design has to be reworked. The clock frequencies used for ADC/DAC are set to 100 MHz for CLK_100 (ADC/DAC SPI process) and 80 MHz for LIO_CLKIN_1 (DUC model). The estimated timing report for the synthesized design meets the time constraints, as shown in Table (2).

Table (2): Estimated Timing Report for DUC model

Constraint	Check	Worst Case Slack	Best Case Achievable	Timing Errors
TS_CLK_100 = PERIOD TIMEGRP "CLK_100" 10 ns HIGH 50%	SETUP	4.412ns	5.588ns	0
	HOLD	0.542ns		0
TS_LIO_CLKIN_1 = PERIOD TIMEGRP "LIO_CLKIN_1" 12.5 ns HIGH 50%	SETUP	5.607ns	6.893ns	0
	HOLD	0.257ns		0

5. FPGA Implementation :

The synthesis output files generated by the ISE software in electronic design interface file (EDIF) and user constraints file (UCF) forms represent the optimized netlist of integrated design, timing constraints, and FPGA pin assignment that have been implemented into the FPGA development board by following the steps listed below:

- Translate: Convert the netlist file of integrated design in EDIF format to native generic database (NGD) file, which contains logic description of hierarchical components and Xilinx primitives for the integrated design using NGD build program.
- Map: Perform logical DRC on the NGD file and map the design logic to slices and input-output (I/O) cells in FPGA to create native circuit description (NCD) file.
- Place and Route: The design in mapped NCD file is place and route into FPGA based on timing constraints using timing analysis tools with no errors found. All signals are completely routed.
- Bit generation and program download: Bit generation is used to generate configuration bit-stream file in BIT format form, and subsequently downloaded into FPGA via JTAG cable using the iMPACT program.
- The timing requirement is satisfied the FPGA requirements.

Finally, the GSM DUC that was designed in System Generator downloaded into Xilinx Virtex-4 FPGA. The simulation result of GSM DUC that has been up converted by 16 to produce IF at 69.333MHz is shown in Figure 12. Clearly shown the output was up sampled into 16 sample rate.

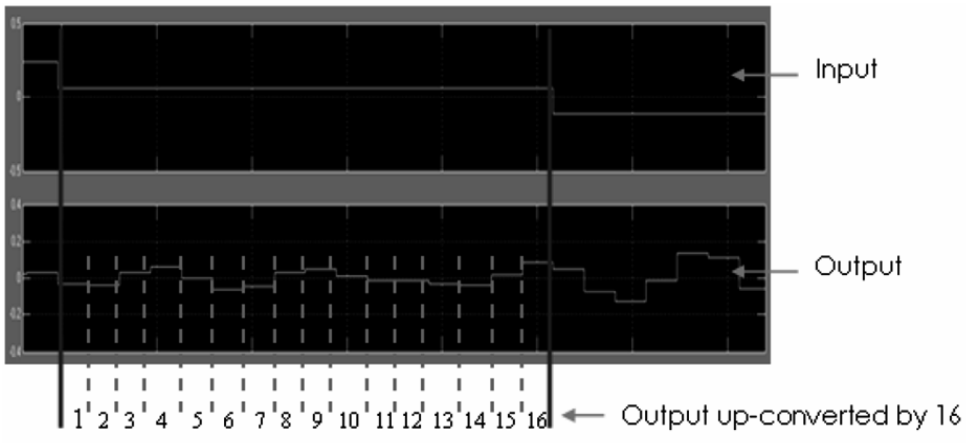

Figure (12): DUC up Converted by 16 factor.

6. Conclusions :

GSM DUC interpolation filter was designed by decomposed the filter into four stages to minimize the used of DSP48 usage. As the conclusion, by minimizing the DSP48 usage, the design can reduce the simulation computational time and reduced hardware complexity. The GSM DUC was successfully design according to Xilinx Virtex-4 FPGA family and fulfilled the GSM requirements as stated in 3GPP TS 25.104 v4.5.0.

7. References :

1. Field-programmable Gate Array Official Website, June 2008, available at:
2. http://en.wikipedia.org/wiki/Fieldprogrammable_gate_array
3. D.B. Chester, “Digital IF Up Conversion for Economical Wireless Implementations”, Southcon/96Conference Record, June 1996, pp. 86-91
4. 3GPP TS 25.104 v4.5.0, BS Radio Transmission and Reception (FDD) Release 4, Association of Radio Industry and Business, June 2002
5. X.Xu, X.Xie, and F.Wang, “Digital Up and Down Converter in IEEE 802.16d”, The 8th International Conference on Signal Processing, vol. 1, pp. 16- 20, 2006
6. Xilinx, Application Notes XAPP1018. Designing Efficient Wireless Digital Up and Down Converters Leveraging CORE Generator and System Generator, October 2007
7. Xilinx, DS558. DDS Compiler v2.0, May 2007
8. Xilinx, Xilinx ISE 9.2i Software Manuals, 2007