DESIGN AND VERIFICATION OF MULTI-RATE DECIMATION FILTER FOR WIRELESS AND MOBILE SYSTEM [+]

Abdulhassan Nasayif Al-Kujaili [*] Aktham Hassan Ali [**] Majid S. Naghmash [***]

Abstract:

This paper present, the design and simulation of multi rate decimation filter to work with wireless mobile system under software defined radio (SDR) technology. The decimation filter is designed with three stages of decimation filter that consists of Cascaded Integrated Comb (CIC) decimation filter, Compensating Finite Impulse Response (CFIR) filter and Programmable Finite Impulse Response (PFIR) filter. The three cascaded filters could operate to reduce the intermediate frequency from 100MHz to 100 KHz baseband signal in order to more processing. System Generator offers the multiplier less Multiply-Accumulate (MAC) Finite Impulse Response block which reduce the implementation area. The three filters are designed and simulated using MATLAB and verified with System Generator design from Xilinx. Results obtained from the simulations and verification of this design, has shown that the proposed algorithm reduces the error to $2x10^{-4}$ between MATLAB design and System generator. The techniques used are promising, and also develops the sample rate conversion of current wireless systems and new generation of wireless communication system up to 100MHz in IF band.

Keywords: DDC, SDR, GSM, MATLAB, System Generator

تصميم مرشح مخمد متعدد السرعات للانظمة اللاسلكية والنقالة

عبد الحسن نصيف الدجيلي أكثم حسن علي ماجد صلال نغيمش

المستخلص :

يقدم هذا البحث تصميم ومحاكات مرشح مخمد متعدد السرعات للعمل مع انظمة الموبايل اللاسكلي بتكنلوجيا الراديوات المعرفة برمجيا. صمم هذا المرشح المخمد بثلاثة مراحل والتي تتضمن المخمد المتعاقب ومرشح التحسين ذو الاستجابة المحدودة والمرشح المبرمج. تعمل المراحل الثلاثة المتعاقبة على خفض التردد المتوسط من 100 ميكاهيرتز الى 100 كيلو هيرتز لغرض معالجة الاشارة الاساسية. يوفر مولد النظام مرشحات لاتحتاج الى عمليات ضرب متكررة والتي تقلل من مساحة التصميم. المراحل الثلاثة صممت باستخدام برنامج ماتلاب وتمت محاكاتها والتحقق منها بواسطة مولد النظام . نتائج المحاكات والتحقق تبين ان هذا التصميم يحقق نسبة خطاء لاتتعدى $2x10^{-4}$بين المحاكات والتنفيذ الفعلي. التقنيات المستخدمة واعدة وتساهم في تطوير عملية تغيير معدل سرعة الاشارة للاتصالات الحالية والمستقبلية لغاية 100 ميكاهيرتز في حزمة التردد المتوسط.

[+] Received on 4/11/2012 , Accepted on 12/11/2013
[*] Professor / Dijilah University College
[**] Assistant Lecturer / Institute of Technology / Baghdad
[***] Lecturer / Institute of Technology / Baghdad

1. Introduction :

In radio communication systems design, the low pass sample IF signal is obtainable to develop the presentation of Analog-Digital Converter (ADC). The purpose of digital front end in transceiver is to decrease the volume and power consumption and facilitate it to have reconstruction capability comparing with analog front end. A complete digital IF demodulation has the benefit to better performance and correctness. Though, with higher sample rate, it's important to decrease the frequency and sample rate in IF band via Digital Down Converter (DDC) filter to reduce the power consumption of the processor [1]. Since wireless communication infra structures have been introduced such as 3G and 4G, Software Defined Radio (SDR) becomes dominant due to its highly configurable hardware and software platforms, as compared to the sophisticated and complicated hardware platforms. Indeed, SDR performs many sophisticated signal processing tasks, e.g. channel estimation, rake receiving, and advanced compression algorithms. There are many silicon solutions for implementing the various functions of SDR, but Field Programmable Gate Array (FPGA) offers the best solution in data rate conversion processing because of its high level of integration (functionality), high performance (speed), high programmability, shorter development cycle, and low development costs [2]. In many SDR systems, decimation part is one of the prevalent methods for data rate conversion [3]. The SDR offers high organize for a diversity of modulation techniques, wide band or narrow band operation. The compensation of SDR systems over conventional wireless communication systems are the flexibility and permit to numerous communication protocols to dynamically performs on the same hardware, thus reducing the cost. Specific functions such as filters, modulation schemes, encoder/decoder could be reconfigured adaptive at run time. This will considerably decrease the cost of the system for both the end user and the service. The essential idea following the software radio is that the analog to digital converter is moved as closed as possible to the antenna and mainly function are realized by digital signal processing. For this reason, the A/D converter operates on extremely high sampling rate. The most important idea of the digital radio receiver is to convert the radio frequency signal into digital baseband signal. This type of receiver could be performed in three stages, convert the radio frequency signal into IF signal digitalized and demodulate it to baseband. This paper discusses the steps to design the decimation filter in the manner of Digital Signal Processing (DSP) by using Matlab/Simulink software [4,5].

The rate conversion is the procedure by which fast frequency data is eliminated from a signal to decrease the sampling frequency with no aliasing. If decimation without filtering were performed, aliasing would occur [6,7] When large changes in sampling rate are required, multiple stages of sample rate conversion are found to be more computationally efficient. Most practical systems employ a multi stage structure, resulting in a considerable relaxation in the specifications of anti aliasing filter in each stage compared to single stage realization. A similar output sequence can be obtained for a given input sequence by inserting a low-pass filter either before or after the decimator. The benefit lies in the investments gained in computational complexity by placing the filter before the down sampler.

The oversampling of incoming signal by a number of orders has to relate to the Nyquist rate. In such case, decimating the signal in a single stage might result in a high cost and inflexible filtering model. A multiple decimation stage could be more efficient technique to implement the sampling rate conversion and the resultant design may achieve the optimum filtering. Furthermore the relation will reduce the number of

multipliers and addresses per second [8,9]. The conventional decimation filter structure shown in Figure 1 could be capable to convert an intermediate frequency band into baseband signal using mixer in the digital region and 2 low pass filters after the A/D converter. In this study, the cascaded integrated comb (CIC) decimator is used with compensating finite impulse response (CFIR) and programmable finite impulse response (PFIR) filters as cascaded decimation filter structure to convert the intermediate frequency to baseband with multiplier less MAC filter available with Xilinx products in order to decrease the multiplications processes. However. The implementation of this decimation filter will consumes less power and decrease the filter size to minimum. As an example, assume the proposed decimator filter is designed to work with GSM mask frequency as well as CDMA system.

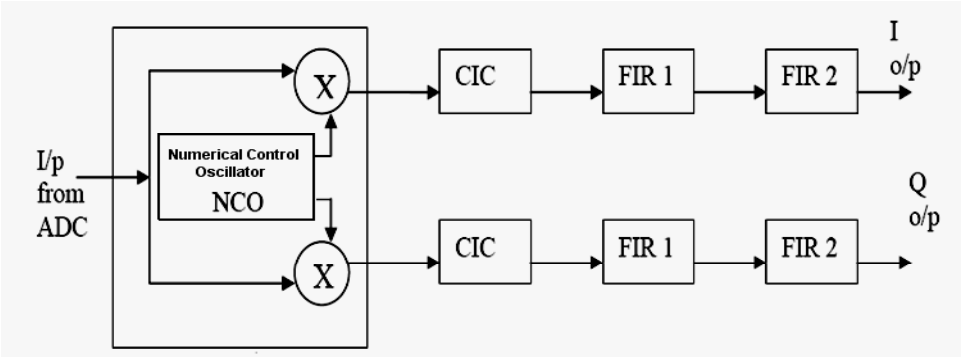

Figure (1): Conventional decimation Filter

2. Decimation Filter Design Using MATLAB -SIMULINK Blocks :

The proposed decimation filter model is designed and simulated in the MATLAB-SIMULINK [4] block to verify the filter performance in the system generator. The filter structures in the SIMULINK block set are shown in Figure 2. The GSM signal is generated by chirp block and filtered down from 69.333248 MHz to 270.833 KHz through the three stages of the proposed filter to recover the GSM signal [6].

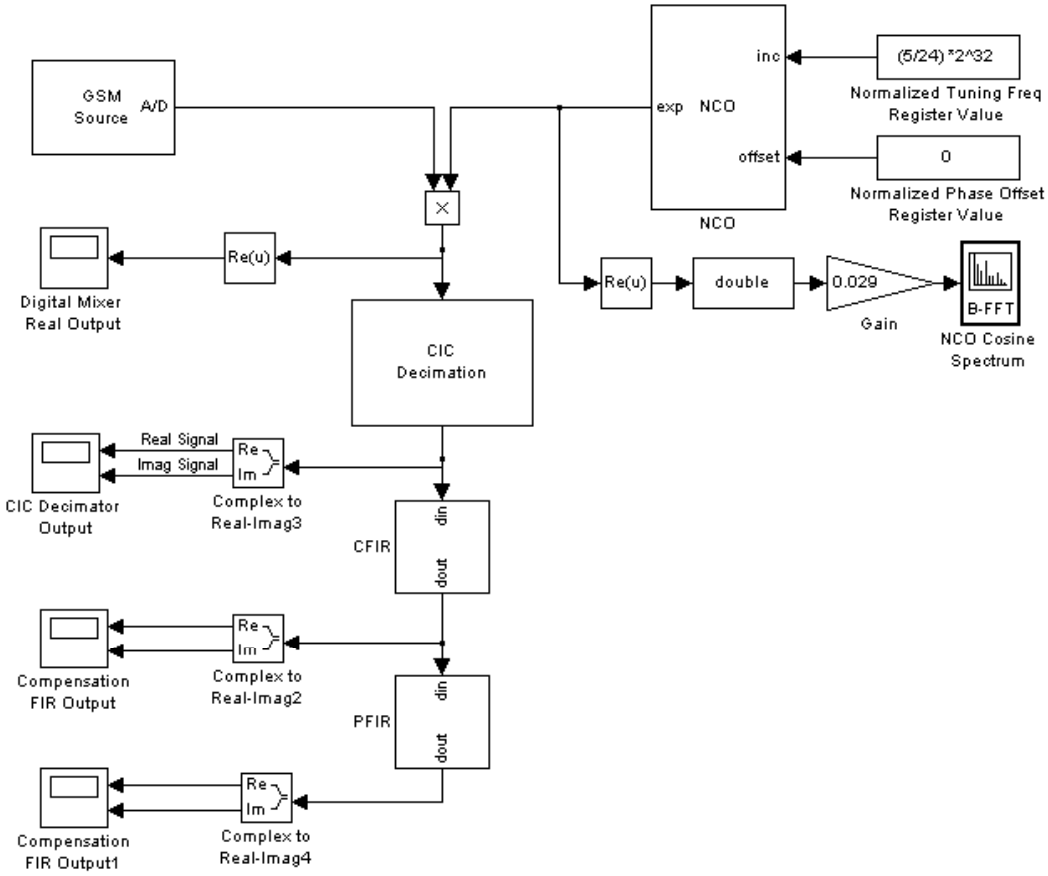

Figure (2): SIMULINK model of proposed decimation filter for GSM mask requirement

The decimation filter chain performs down-conversion of the input signal as well as narrow band low-pass filtering and decimation. The designed filter produces low sampling rate of 270 KHz baseband signal, which signifies that the signal is ready for demodulation. The parameters of blocks in the filter chain have been modified to facilitate observation of the possibilities for modeling a customized decimation filter with SIMULINK. The GSM source block in the model is used to switch between a chirp and sinusoid signal. Accordingly, the parameters of the NCO block have been adjusted. The frequency and phase have been adjusted to 32-bit tuning frequency register value and 16-bit phase offset register value as input to the NCO block. The five-stage Cascaded integrated comb (CIC) filter with 64 decimation factors down converts the GSM intermediate frequency (IF) to lower rat as a first stage. The second stage is the adjustment of the roll-off of the CIC baseband with a 21-taps compensating Equiripple FIR filter (CFIR). Composing the closing stage of filtering and shaping of the required GSM signal using a 65-tap PFIR filter compos the final stage. Chirp signal shown in Figure 3 have a sampling rate of Fs = 69.333248 MHz and period sample of Ts = 14.4 ns, which are processed by the DDC filter according to the GSM requirements. The three stages decimation filter design and simulation are explained in following sub-section.

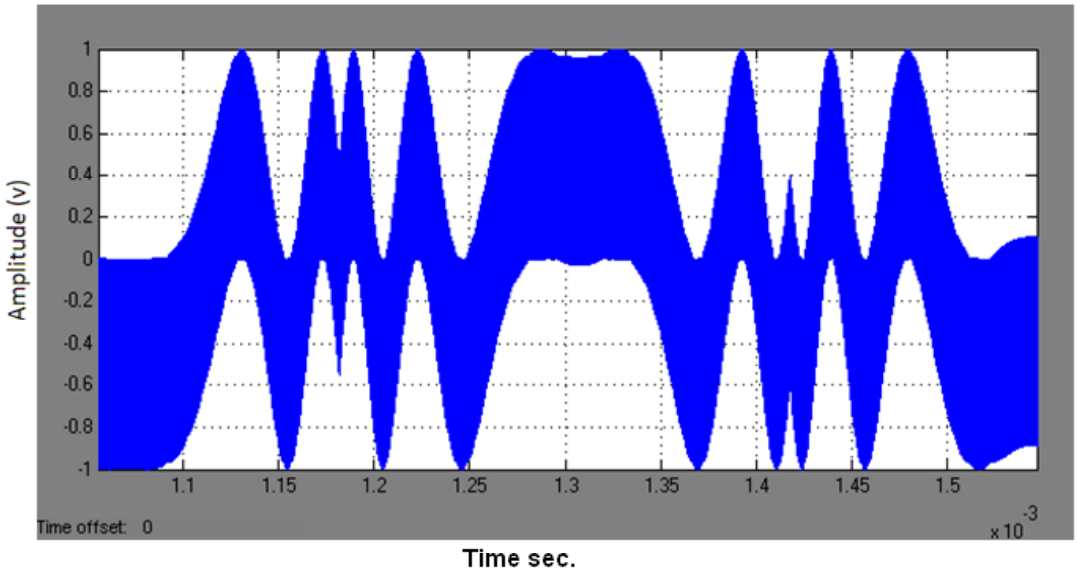

Figure (3): Chirp signal of GSM intermediate frequency (IF) 69.333 MHz

2.1 CIC Filter Design Using SIMULINK Block Set :

The input chirp signal of 69.333248 MHz is down converted by the five-stage CIC filter with decimation factor of 64 and a rate change of 256 / 64 = 32. The output signal of the CIC filter appears similar to GSM signal in terms of shape but with different sampling frequency of 1.0833 M sample/sec., as shown in Figure 4. The CIC filter response resembles either the upper or the lower envelope of the mixed signal but down-sampled by 32. The envelope is extracted by the CIC filter with a decimation factor of 64 and normalization gain of 2^{30}. Furthermore, the peak values of the CIC filter response are maintained at ±0.5, which is equal to the envelope of the mixed signal. However, the sample rate of the CIC filter response is 32 times lower than the sampling frequency of 69.333248 MHz

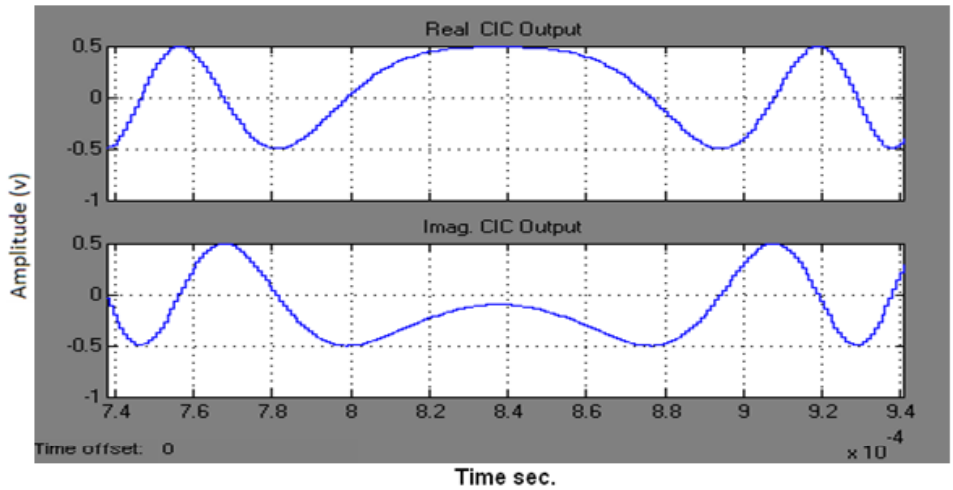

Figure (4): First stage CIC filter response

2.2 CFIR Filter Design :

The implementation of CFIR starts with designing the filter coefficients in fixed point values using MAC FIR decimator in System Generator as shown in Figure 5.

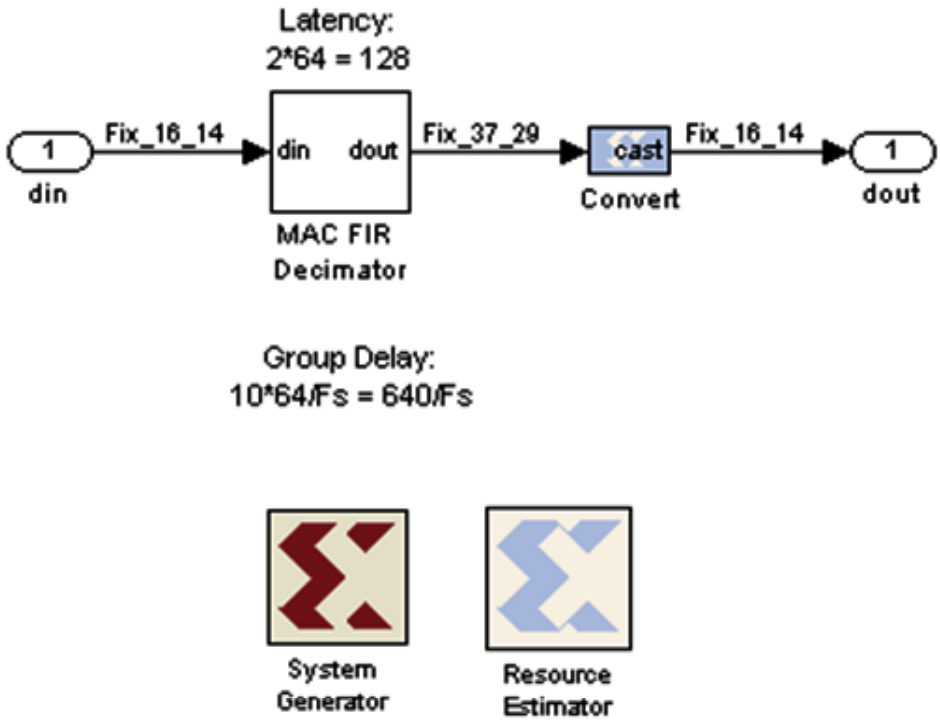

Figure (5): MAC CFIR Decimator

For the CFIR filter design, the FDATool digital filter design window has been used. The response type is set to LPF and the design methods are set to Equiripple, with respect to the design approach. The filter order is set to 20 (21-taps) and the sampling frequency is set to 1.083332 MHz. Therefore, the sampling period of CFIR filter is 64Ts = 923.0781 ns, which satisfies the timing constraints of MATLAB SIMULINK block set. The cut-off frequency is set to 0.09 MHz for the design optimization. Default value of density factor is set to 20, representing a reasonable trade between the accurate approximation to the ideal filter and the time required to design the filter. The output magnitude response indicates that the filter is providing the required band and filter information window, which in turn, proves that that the filter is stable. The linear phase in the band of interest is shown in Figure 6. The resulting signal appears more close to the GSM signal in shape but different in sampling frequency, as shown in Figure 7. Therefore, this signal needs more filtering process to achieve the exact GSM signal in the next stage.

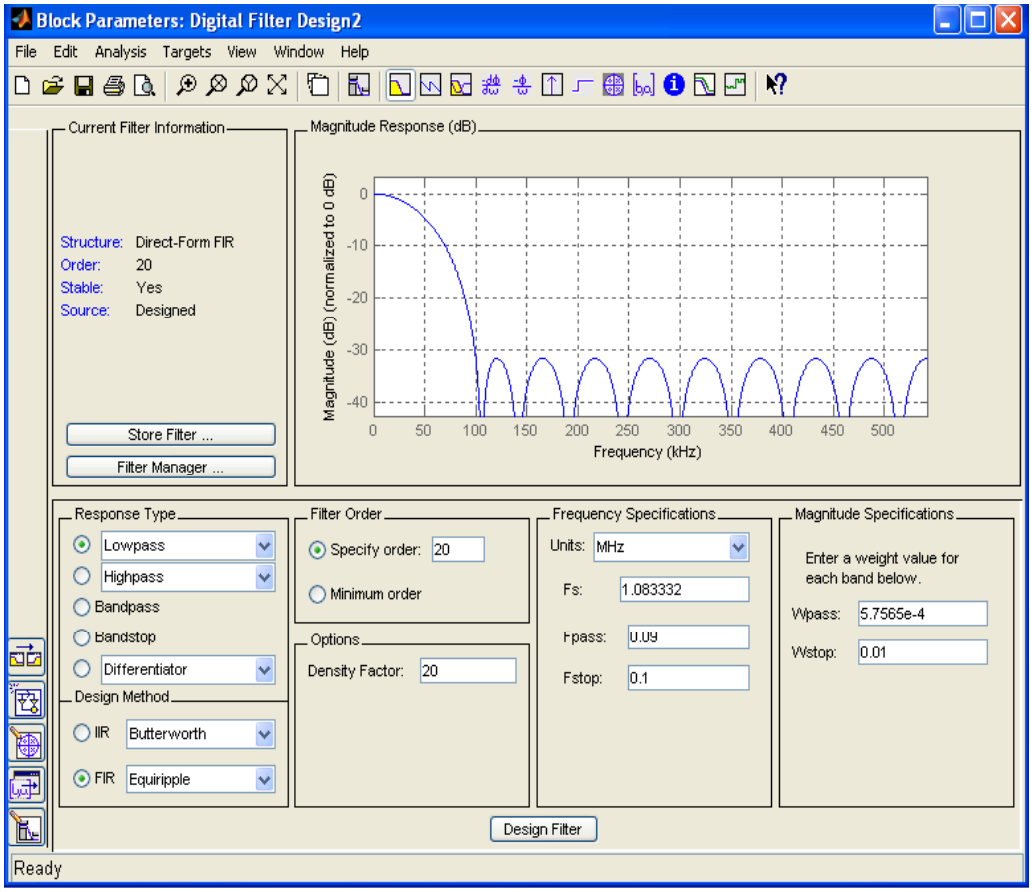

Figure (6): Magnitude response of CFIR filter

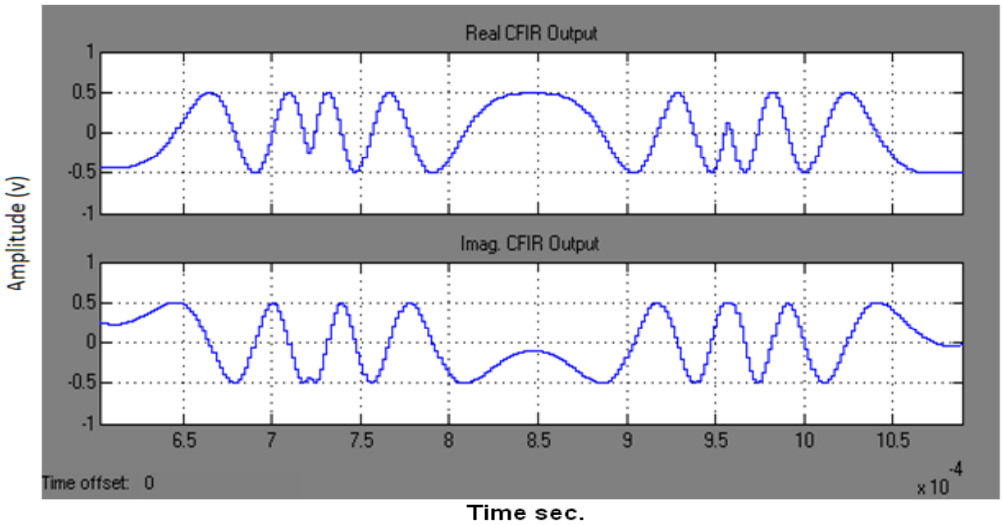

Figure (7): CFIR output signal

2.3 PFIR Filter Design :

The PFIR filter coefficients have been designed in fixed point values using the FDATool provided by MAC FIR decimator in System Generator as shown in Figure 8. The designed filter is connected in parallel with the floating point MATLAB design to verify the PFIR filter coefficients before implementation in real time.

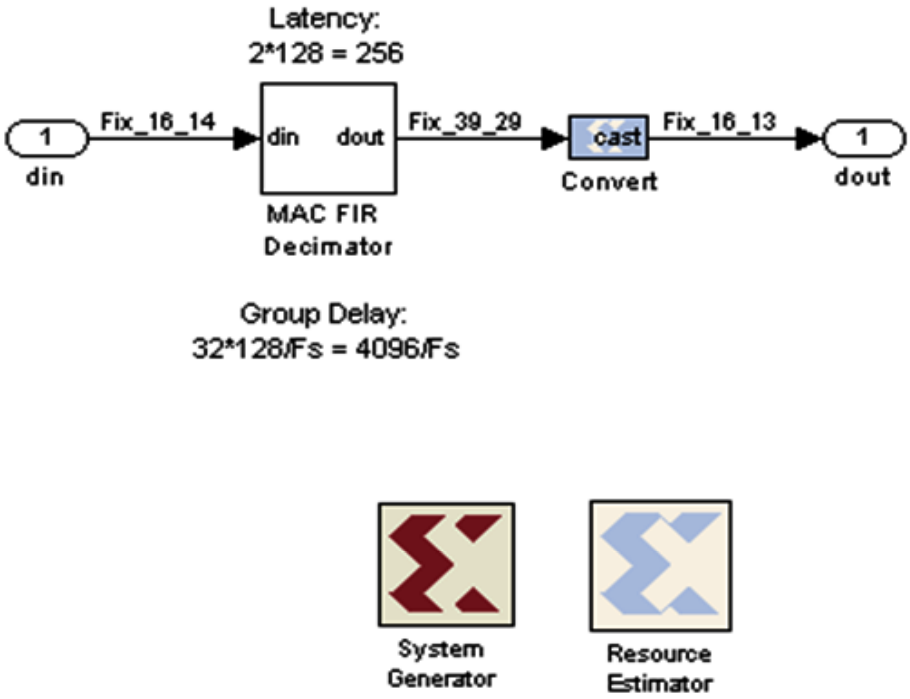

Figure (8): MAC PFIR Decimator

In designing the PFIR filter, the FDATool digital filter design window has been used. The response type is set to LPF and the design methods are set to Equiripple with respect to design approach. The filter order is set to 64 (65 taps), and the input sampling frequency of the PFIR filter is set to 541.666 KHz. The sampling period of the PFIR filter has been set to 128Ts= 846.1561 ns to satisfy the timing constraints of MATLAB SIMULINK block set. The cut-off frequency is set to 0.08 MHz which is representing the desired band for the GSM system. A default value density factor is set to 20, representing a reasonable trade between the accurate approximation to the ideal filter and the time needed to design the filter. The magnitude response indicates that the filter is providing the required band and the filter information window proves the stability of the filter. The linear phase in the band of interest is shown in Figure 9.

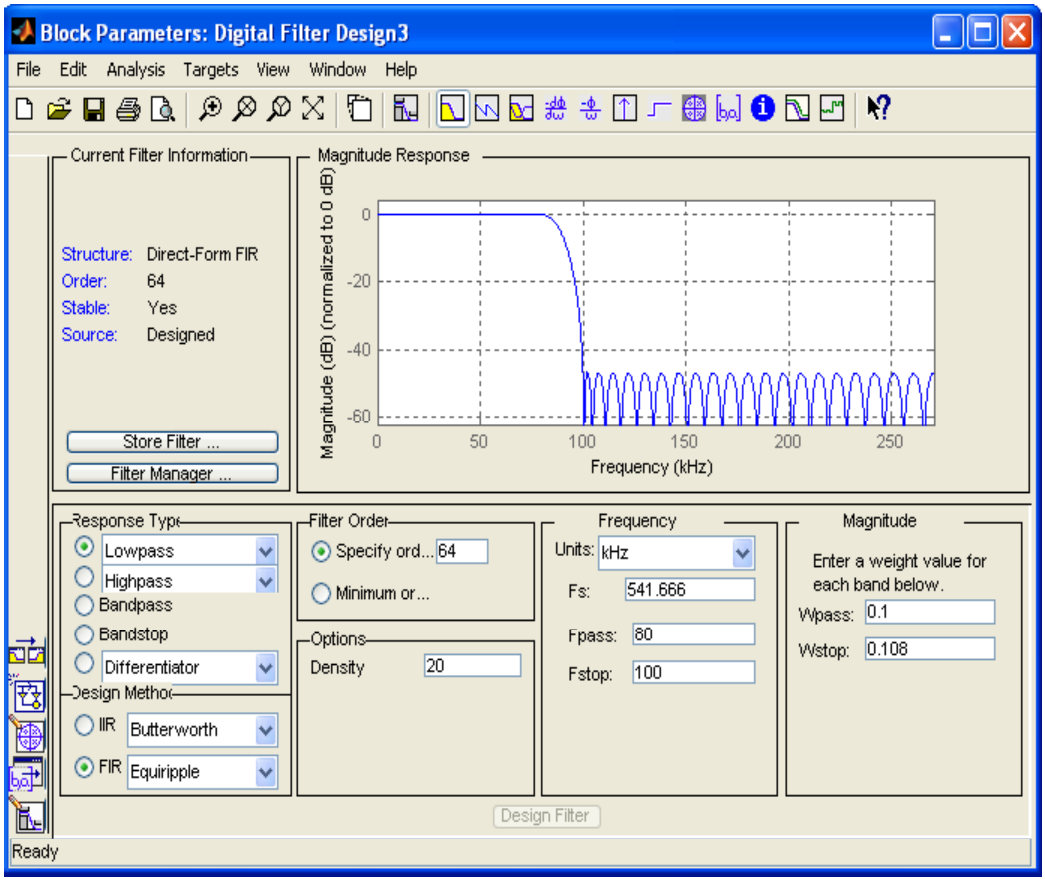

Figure (9): Magnitude response of PFIR filter

The resulting signal appears exactly similar to the GSM signal with respect to shape and sampling period. Hence, the output sampling period is 256Ts=3692.3122 ns and the output sampling frequency is Fs = 1/3692.3122 = 270.332 KHz, as shown in Figure 10. Therefore, the three-stage DDC filter satisfies the GSM requirements in the SIMULINK model

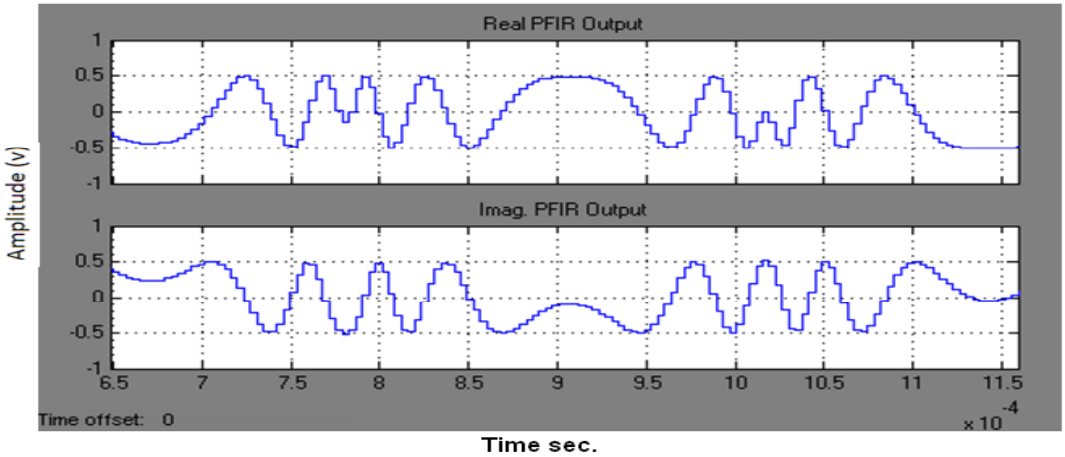

Figure (10): PFIR output signal

3. Overall Decimation Filter Design Using Fixed Point Values :

The combined decimation filter structure contains CIC, CFIR, and PFIR, which are connected in the System Generator to verify the filter performance with the MATLAB design. The filter structure is shown in Figure 11.

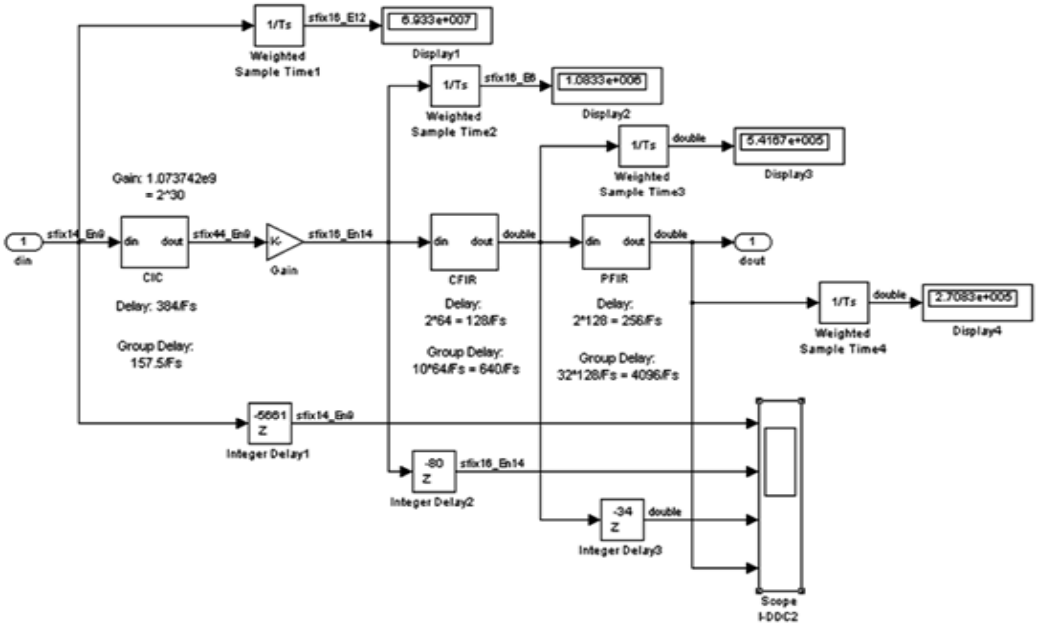

Figure (11): Decimation filter structure of 3-stage

The resulting response for combined filters in the System Generator is shown in Figure 12. The mixing of chirp and sinusoidal signals in fixed point value as input of the decimation filter and the filter responses at each consecutive stage in the filter chain is synchronized. This is achieved by imposing delays upon the CFIR filtered signal, normalized CIC filtered signal, and mixed signal at (4096 + 256) = 4352, 4352 + (640 + 128) = 5120, and 5120 + (157 + 384) = 5661 unit sample time, respectively, where 1 unit sample time = $(69.333248 \times 10^6)^{-1}$ ns = 14.423095 ns. The first and second terms in parentheses are the respective group and processing delays of the PFIR, CFIR, and CIC filters in the proposed DSP filter chain.

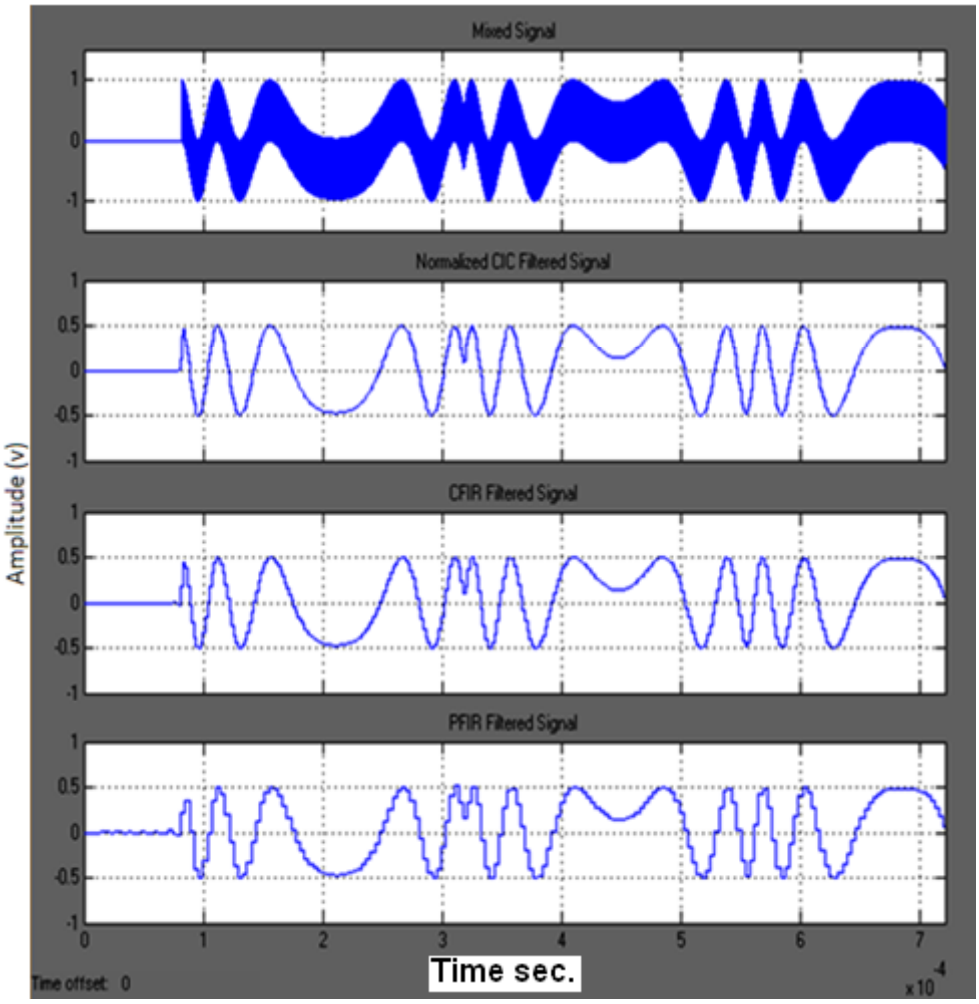

Figure (12): Ideal decimation filter response

The decimation filter response resembles either the upper or the lower envelope of the mixed signal although it is down-sampled by 256. Down-sampling is obtained because the envelope is extracted first by the CIC filter with a decimation factor of 64 and normalization gain of 2^{30}, subsequently by the CFIR filter with a down sampler of 2, and finally by PFIR with a down sampler of 2. Furthermore, the peak values of the DDC filter response maintained at ±0.5 is equal to that of the envelope of the mixed signal. However, sample rate of the DDC filter response is 256 times lower than the sampling frequency of 69.333248 MHz.

4. Decimator Design Using Floating Point Values :

The three stages of the decimator filter in floating point design contain CIC, CFIR, and PFIR, which are combined in the System Generator, as shown in Figure 13.

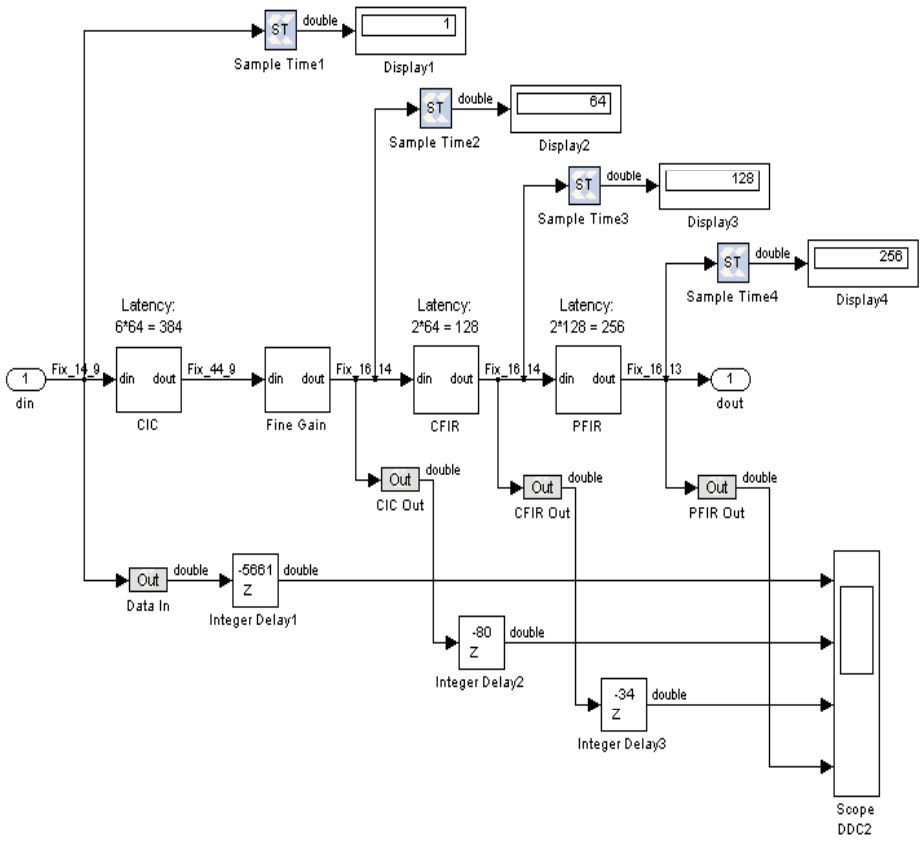

Figure (13): decimator design in floating point values

The resulting response of this structure is shown in Figure 14. The mixing of chirp and sinusoidal signals in fixed point value as input of the proposed filter and the filter respond at each consecutive stage in the ideal decimator, starting from the stage of normalized gain with CIC filter at fixed point values to the CFIR and PFIR filters at floating point double-precision values. In Figure 14, the decimation response is shown to clearly resemble either the upper or the lower envelope of the mixed signal although it is down-sampled by 256. The envelope is extracted first by the CIC filter with a decimation factor of 64 and normalization gain of 2^{30}, subsequently by the CFIR filter with a decimation factor of 2, and finally by PFIR with a decimation factor of 2. Furthermore, the peak values of the decimation filter response maintained at ±0.5 is equal to the envelope of the mixed signal. However, the sample rate of the DDC filter response is 256 times lower than the sampling frequency of 69.333248 MHz. The three-stage decimation filter (CIC, CFIR, and PFIR) response produces the exact shape of the GSM signal in the individual stage.

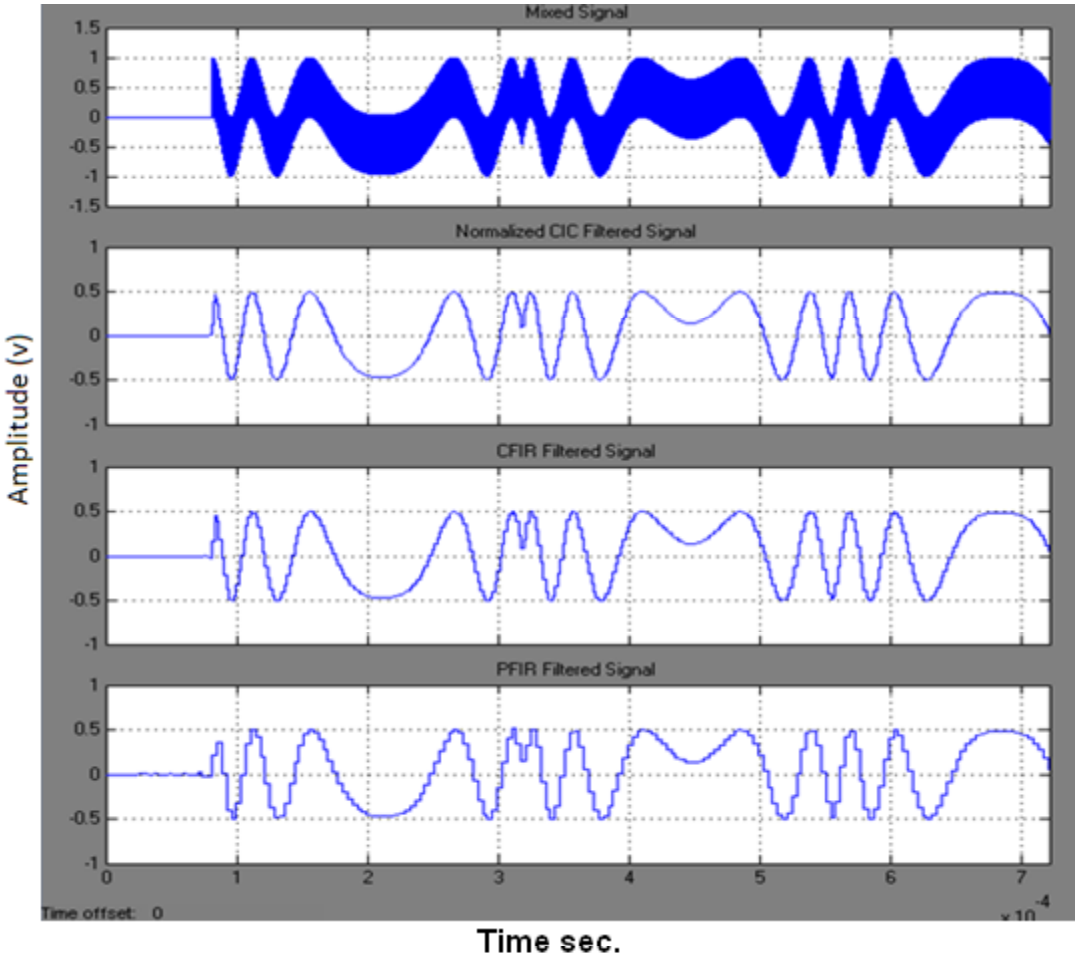

Figure (14): Proposed Overall decimation Response

5. Verification of Overall Decimator Filter Design :

According to [10] and the study of [7], [8], [9], [11], the complete decimator structure in fixed point values is verified with floating point values of the decimation filter as an initialization process before running the System Generator simulation in the implementation process. This establishes the correct configuration for the operation of the System Generator model, as shown in Figure 15. The response of the combined cascaded filter is shown in Figure 16. The simulation result shows that the difference between the fixed point design and floating point decimator response is less than 2×10^{-4}. This is mainly because of the quantization errors resulting from the limited number of bits representing the numerical values used in the arithmetic functions such as multiplication and summation in filtering process. In this case, the inputs and outputs of the CFIR and PFIR filters are set to fixed point values of 16 bits and 14^{th} binary point. Nevertheless, the difference value below 2×10^{-4} can still be accepted as valid accuracy, as long as the proposed decimator response closely resembles the ideal response and does not jeopardize the performance of the subsequent processing after decimation part.

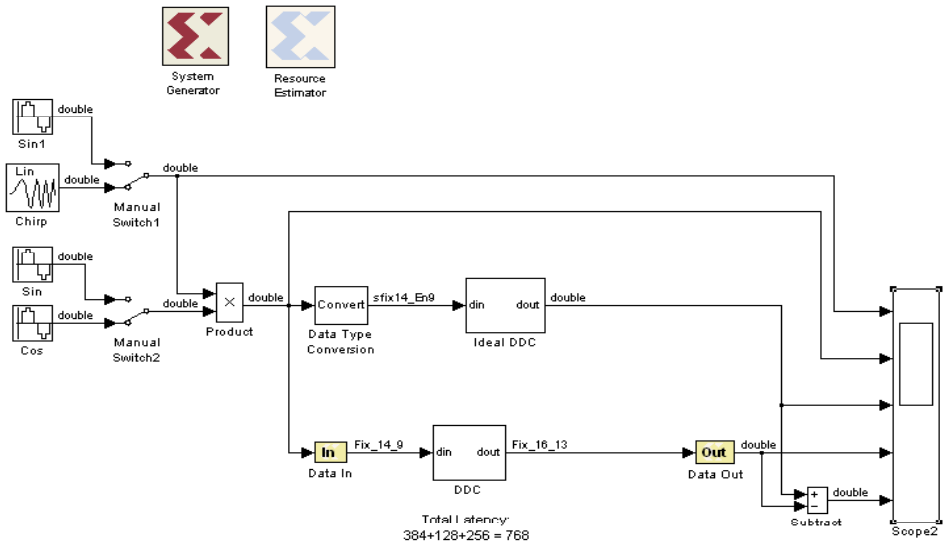

Figure (15): Verifications of Decimator Design

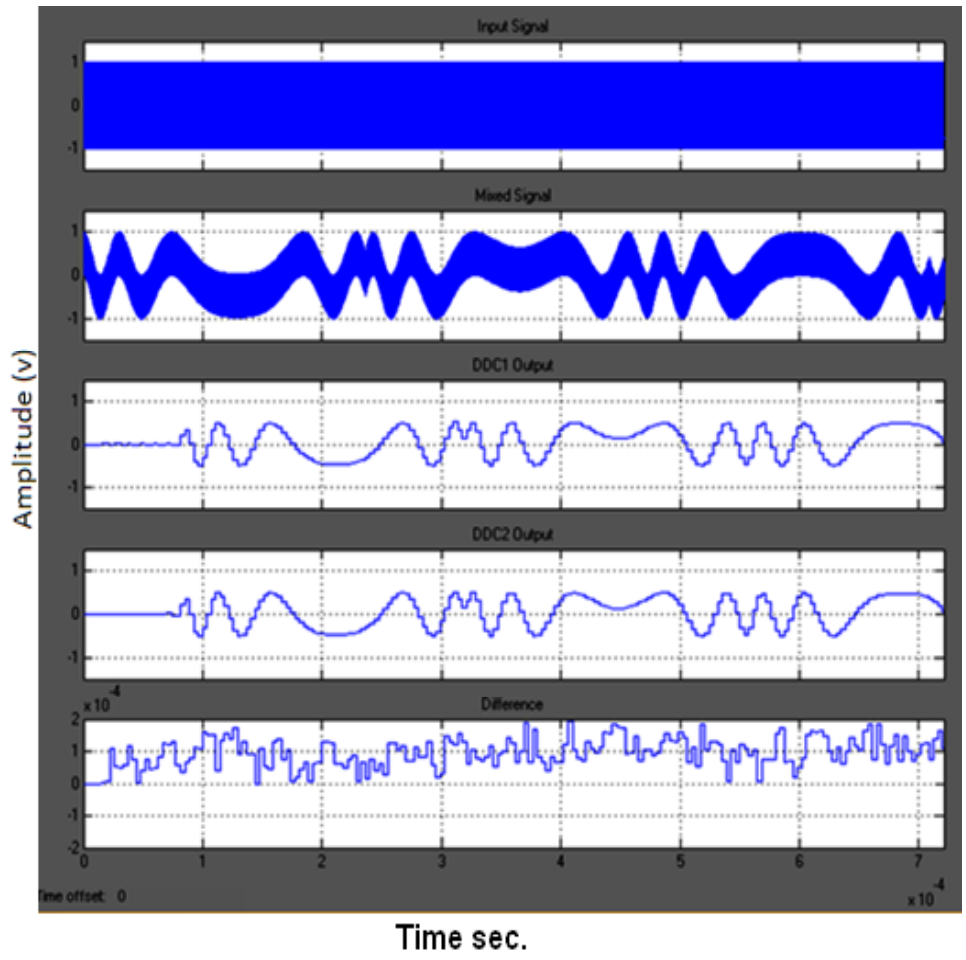

Figure (16): Response of the combined cascaded filter

6. Conclusion :

This paper presents a detailed guideline to design and simulate the multi-rate decimation filter for wireless mobile system. A lot of software and design tools have been used to verify the design output in terms of functionality, synthesis, timing, and area constraints. The similarity of simulation in MATLAB and system generator result shows the success of reducing the error between two type of software simulation will be further used for up-conversion through external analog system. A tradeoff between the number of stages and complexity was provided to implement a 3-stage decimation filter for mobile system. To realize this technique, two filters has been utilized, they are, Compensation Finite Impulse Response (CFIR) filter and Programmable Finite Impulse Response (PFIR) Filter The proposed filter algorithm could be considered as the talented algorithms for the Software Radio applications due to its less complexity and low power consumption. The design of decimation filter could be further tuned to provide a less complexity to implement with multi-standards over the communication systems. Meanwhile, the decimation filter should be designed with better impulse and frequency response, so that the performance of receiver could be further improved.

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