DYNAMICALLY RECONFIGURABLE LOW POWER CONSUMPTION ADAPTIVE VOLTAGE CONTROLLED OSCILLATOR USING FPAA [+]

تشكيل هزاز فعال تكيفي ذو استهلاك منخفض للقدرة مسيطر عليه بواسطة الجهد

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Abstract:

This research presents the possibility of using field programmable analog arrays in designing and executing a voltage controlled oscillator circuit. Field programmable analog arrays are distinguished for including all the mutual components necessary for processing analog signals. AN221E04 chip, the specification of which has been explained in this research, has been used in building up an advanced voltage controlled oscillator circuit. This circuit is distinguished for its simplicity, high stability degree, low power consumption, small size; in addition to decreasing the noise effect on the output circuit. Simulation of the proposed circuit has been completed according to Anadigm Designer2 software, and simulation results were shown on a programmable signal drawer, and the results were identical, which reflects the competency of the software used in the circuit.

Keywords - chirp, chaotic, QPSK, spread spectrum.

المستخلص:

يقدم البحث إمكانية استخدام تقنيات المصفوفات التشابهية القابلة للبرمجة في تصميم وتنفيذ دارة هزاز متحكم به عن طريق الجهد. تمتاز المصفوفات التشابهية القابلة للبرمجة باحتوائها على جميع المكونات المشتركة الضرورية لمعالجة الإشارات المتناظرة. تم استخدام رقاقة (AN221E04) والتي تم شرح مواصفاتها في هذا البحث في بناء دارة هزاز متحكم به عن طريق الجهد مبتكرة. تمتاز هذه الدارة بالبساطة، درجة استقرار عالية ،استهلاك منخفض للقدرة، صغر الحجم إضافة الى تقليل تاثير الضجيج على إشارة الخرج. تم إجراء محاكاة للدارة المقترحة وفق برمجيات (Anadigm Designer2) وعرضت نتائج المحاكاة على راسم إشارة برمجي، وقورنت النتائج مع مثيلاتها المعروضة على راسم إشارة مخبري وكانت النتائج متطابقة مما يدل ذلك على كفاءة البرمجيات المستخدمة في المنظومة.

Introduction:

Sinusoidal oscillators play a very important role in most of the electronic systems viz, in instrumentation and control systems etc. VCOs are useful in frequency-modulated transmitter where the music or voice signal must cause the transmitted carrier frequency to vary in step with the signal amplitude and also in the tuner of any television receiver with pushbutton tuning [1]. The VCO circuit is a fundamental part in a PLL system. It could provide a

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controllable and stable frequency signals for the system, so it has wide application in the electronic measurement equipments. At present, the most frequently used VCO circuit fabricated in CMOS process is LC oscillators and ring oscillators. Although LC oscillators perform well in phase noise suppression, it also have many disadvantages, such as large layout area, the difficulty of designing inductance with a high Q value in present CMOS process, and a narrow tuning range etc [2]. VCO can be classified into three topologies, ring topology, relaxation topology, and the harmonics one as shown in Fig. 1. In a relaxation oscillator, the oscillation relies on nonlinear switching that charges and discharges a capacitor with a time constant. The oscillation frequency is tuned by varying this time constant. It is usually limited to moderate frequencies. Ring oscillators are normally designed by cascading an odd number of inverters in a loop. A variable resistor or current source is used for tuning. The frequency range can also be adjusted by digitally adding or removing inverters from the chain (coarse tuning). Although Ring and relaxation oscillators have advantages, such as highly integrated in VLSI, low power, small die area occupancy, and wide tuning range, it suffer from a poor frequency stability, which cause a higher noise. On the other hand, harmonic oscillator has an outstanding noise and jitter performance at high frequency. However, it suffers from its inherently narrow tuning range, and the integration of LC-based is more costly due to the large space allocated to on-chip inductors [3]. Most of the disadvantages can be avoided by using FPAA.

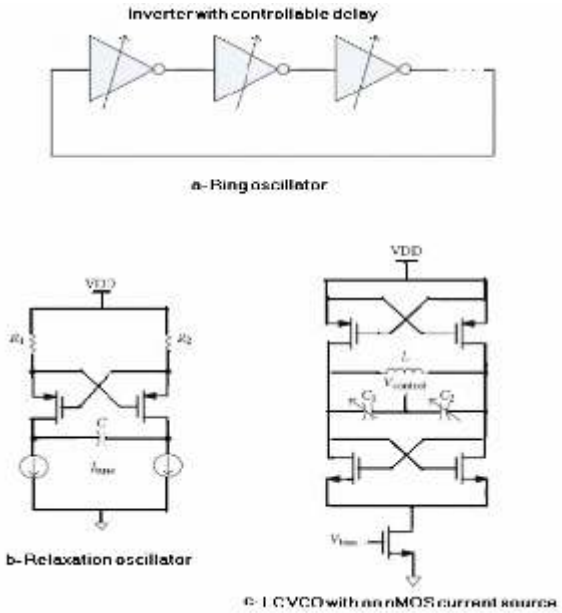

Fig. 1. Voltage Controlled Oscillator topologies

Field Programmable Analog Arrays (FPAAs) are analog integrated circuits based on configurable analog blocks and programmable interconnections. They provide to the analog world the same flexibility as their digital counterparts, Field Programmable Gate Arrays (FPGAs), provide to digital circuits. They allow fast prototyping and offer some interesting features for applications such as adaptive control and instrumentation and evolvable analog hardware [4]. The programmable analog circuit, can be used universally understood by the program configured for circuit see Fig. 2 . FPAAs can be used for the realization of different functional units, circuits, circuit elements. These circuits can be used effectively in applications where the low electric power, the lower development and component cost, the

effective electronic CAD possibility are important. The advantage of FPAAs in the field of faster and more economical circuit planning is significant. It is beneficial in self-developing circuit applications, in neural networks, in signal conditioning, in filters, in fuzzy controls and high frequency applications . According to other approaches FPAAs serve the linear and non-linear implementation of the analog system and the scalability of the application to be realized [5].

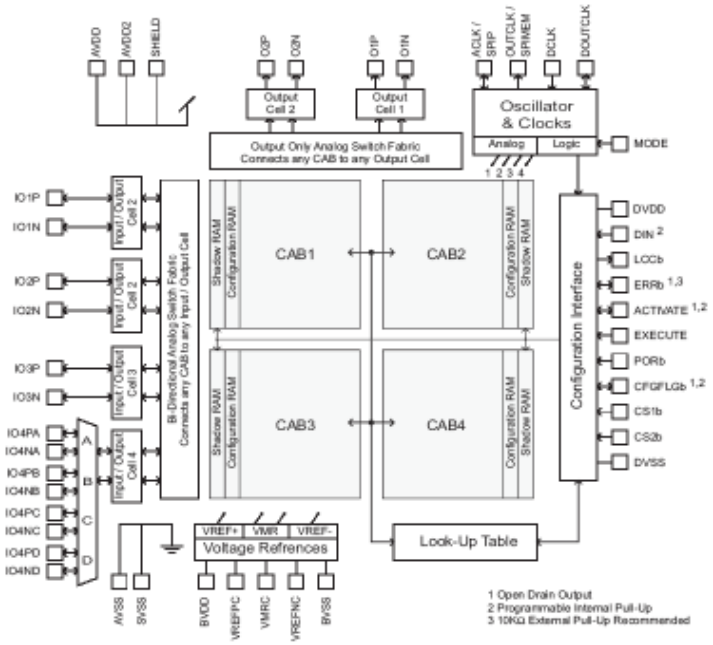

Fig. 2. Internal structure of most popular Anadigm's FPAA with the four configurable analog blocks.

Advances in reconfigurable analog technologies are allowing field-programmable analog arrays (FPAAs) to dramatically grow in size, flexibility, and usefulness. With these advances, analog circuits and systems can be programmable, reconfigurable, adaptive, and implemented on standard CMOS to take advantage of scaled CMOS technology, exhibiting a density comparable to digital memories [6].

In this paper, An approach for a simple, fast and economical VCO technique which uses one Field Programmable Analog Arrays (FPAAs) is described. The primary advantages of this approach include: minimizing the design and development time for constructing the circuit, minimize the effect of the noise and combines the advantages of low power, and high speed.

This paper is organized as follows: In Section 2 of this paper the FPAA Technology are discussed. Section 3 describes the Voltage-Controlled Oscillator. Section 4 presents the an effective method for the implementation of hardware VCO. Section 5 concludes this work.

The FPAA Technology:

By the end of the last decade a new type of analog circuit, based on configurable blocks, was introduced to the market: the Field Programmable Analog Arrays (FPAAs). The FPAAs provide to the analog world the same advantages as their digital counterparts, the Field Programmable Gate Arrays (FPGAs), provide to digital circuits such as reconfigurability and fast prototyping. As FPAAs become an important platform to analog circuit design, it is important to ensure the fault-free condition of these devices as well as the correctness of the user programmed functions [7].

FPAAs are VLSI devices built on operational amplifiers, capacitors, switches, and static

RAMs integrated onto the same silicon chip. Once the application circuit topology has been fixed, capacitance values can be modified by the user altering their values in the RAM array. Thus, taking advantage from the switching capacitor technology, a wide variety of analog blocks with varying specifications can be realized by only changing capacitance values. The FPAA configuration is performed by means of a proper development environment, in which the user can draw the desired analog circuit and send the related data block to FPAA device through RS232 communication. The received data are then stored by the FPAA in the RAM, in order to properly set the internal capacitance according to the designed analog circuit . The reconfigurability makes FPAAs a very powerful tool in circuit design and testing, since they allow obtaining a large number of different transfer functions, without the need of manually assembling the circuit. In particular, the main advantage relies on the opportunity of easily reprogramming the chip: so that the capacitance values inside FPAAs can be varied quickly in order to dynamically change the characteristics of the implemented analog blocks (i.e., CAMs) [8].

The VCO generator prototype was realized in the PAM-5000R FPAA chip of AN221E04 shown in Fig. 3. This AN221E04 chip consists of four configurable analog blocks, each of which contains op-amps, a comparator, and switched-capacitor arrays, integrated with an analog switch fabric.

Configurable analog modules, such as inverters, adders, multipliers and integrators, are implemented easily due to system/block level design instead of transistor level design. The analog circuits are fully differential within the chip but differential-to-single/single-to-differential ended converters are provided on the evaluation board that hosts the chips to access the outputs/inputs of the chips, respectively. There is also an 8-bit look-up-table available for arbitrary transfer functions. The switching of the capacitors are controlled by a system clock whose frequency can also be controlled to a certain extent. The basic principle of the available modules is to sample their input(s) at specific phases of the system clock and provide the corresponding output at the same phase or at some other phase of the clock. For example, the multiplier samples its inputs at phase φ_1 (voltage-high phase of the clock) and outputs the corresponding multiplication at the next φ_1. The look-up-table, similar to the multiplier, results in one system period (inverse of system clock frequency) delay. Thus latencies exist among the blocks computing different variables of the system [9].

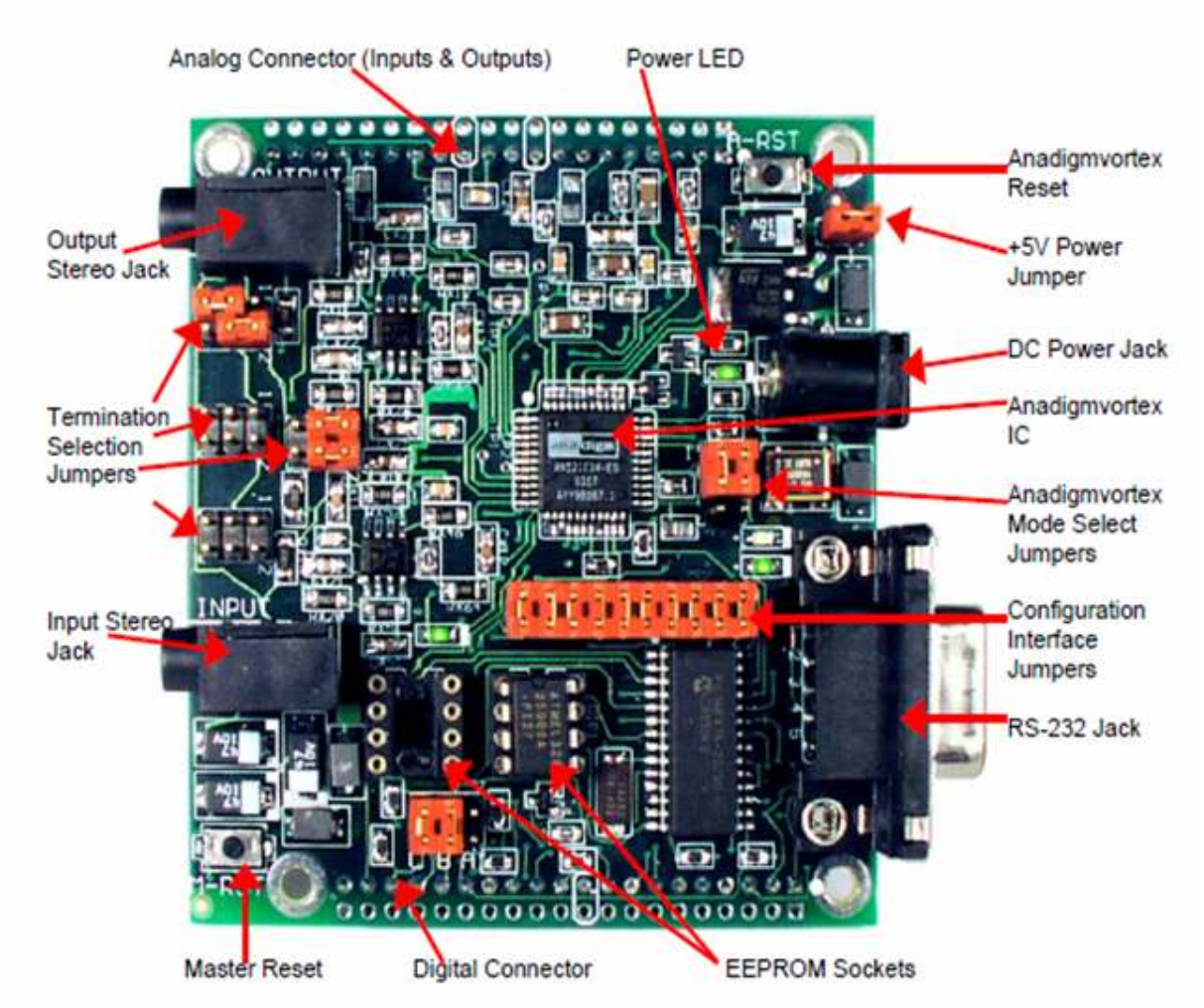

Fig. 3. PAM-5000R FPAA chip of AN221E04

One of the main reasons in choosing the chip of AN221E04 is the dynamic reconfiguration capabilities provided. Once the chip is loaded with a primary configuration subsequent update configurations can be sent to the chip from an external source, which modify only part of the circuit in real time. This process is made possible through the use of shadow and configuration SRAM banks. Configuration data received at the chip is stored in shadow SRAM and once the complete data set has been received, the configuration data is loaded into configuration SRAM in a single clock cycle. This enables on-the-fly circuit update possible without interrupting operation of the FPAA, thus maintaining system integrity. Another good feature, which is provided with the Anadigm Designer 2 EDA tool, is the automatic creation of a software API which allows remote control over a circuit implemented on the FPAA from a PC or microcontroller. The functions provided with the API generate the specific reconfiguration data needed to modify certain parameters of CAM's in a design. In the past, on-line parameter update and partial reconfiguration has been a difficult task with analogue device. However, the dynamic reconfigurability of the AN221E04 device makes it possible to perform on-line parameter update for a circuit implemented on the FPAA [10].

Voltage-Controlled Oscillator:

In this section we will study a behavior modeling of VCOs. The output frequency of the VCO is [11]:

$$\omega(t) = \omega_0 + G_{VCO}\ U_{in}(t) \qquad (1)$$

In (1) the G_{VCO} is defined as:

$$G_{VCO} = \frac{d\omega}{dU_{in}} = 2\pi \frac{df}{dU_{in}} = 2\pi\, g_{vco}$$

where $U_{in}(t)$ is the input signal to the VCO, G_{VCO} is the VCO's voltage-to-radian frequency gain in radians per second per volt and g_{VCO} is the VCO's voltage-to-frequency gain in hertz per volt. When $U_{in}(t)$ = 0, the VCO oscillates at some initial frequency, ω_0, called the frequency offset or free-running frequency.

Consider a sinusoidal voltage with amplitude U_a, argument $\varphi(t)$, and DC offset U_{off}:

$$U_{vco} = U_a \sin\left(\varphi(t)\right) + U_{off} \qquad (2)$$

The argument $\varphi(t)$ is the time integral of the angular frequency:

$$\varphi(t) = \int \omega(t)dt + \varphi(0) \qquad (3)$$

Assuming ω is constant and substituting $\varphi(t)$ in $u(t)$ yields the well known form:

$$U_{vco} = U_a \sin\left(\omega t + \varphi(0)\right) + U_{off} \qquad (4)$$

If ω is not constant, the general form is:

$$U_{vco} = U_a \sin\left(\int \omega(t)dt + \varphi(0)\right) + U_{off} \qquad (5)$$

Replacing $\omega(t)$ with (1) and considering $\varphi(0)=0$, we obtain the VCO's transfer function:

$$U_{vco} = U_a \sin\left(\int (\omega_0 + G_{VCO}\ U_{in}(t))\, dt\right) + U_{off} \qquad (6)$$

After the modification of the (6) we finally get the form:

$$U_{vco} = U_a \sin\left(\omega_0 + G_{VCO} \int U_{in}(t)\, dt\right) + U_{off} \qquad (7)$$

Eq. 7 is the basic equation for the VCO's time-analysis modeling.

The Circuit Design and Experimental Results of The VCO Circuit:

The research aims at designing and executing a voltage controlled oscillator circuit created

by using the field programmable analog array techniques, which are very modern techniques that show high flexibility in performing the different analog circuits. They are mostly used in analog circuits applications that require using high accuracy components, as it was the practice in traditional techniques. It is also possible to change these parameters upon request during the operation of the specified circuit. Building up some circuits of high credibility necessitates multiple secondary circuits through one circuit, each of which has its own parameters, in addition to the limited required volume. Field programmable analog arrays provide a practical solution with a high rate of credibility in solving all those problems. Systems used in using such techniques are subject to a control circuit and central follow up by software's prepared for this purpose. It is possible, by using these techniques, to perform a lot of complex circuits software's through the software circuits that such techniques have.
The user-defined voltage transfer function unit, which is made available by the component box of the AN221E04 chip, has been used in designing and architecting the voltage controlled oscillator circuit, as shown in Fig. 4 (FPAA 3).

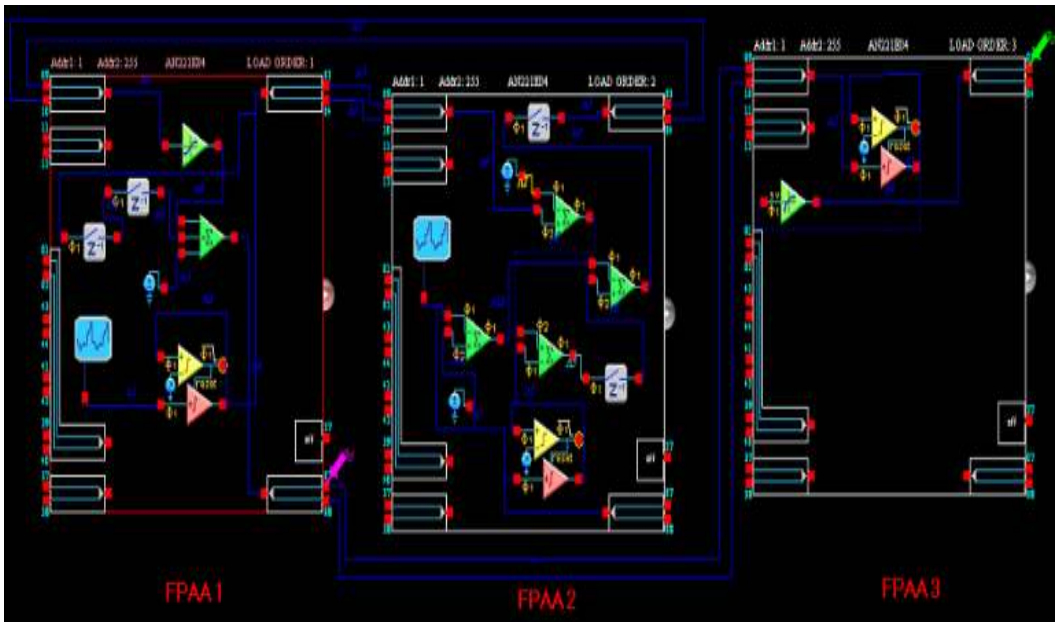

Fig. 4 Ramp signal and VCO Generator.

This unit is distinguished for containing the lookup table (LUT), through which this unit programming is performed by a signal of time-specified specifications, frequency, and amplitude; in addition to a number of samples that represent a complete signal cycle. This block has been programmed with a sine signal of a time period that equals a single bit time of the digital statements, which can be calculated from the following mathematical relation [12]:

$$M.N = \frac{T_p}{16 * T_{Master}} \tag{8}$$

where M is a factor whose value determines the value of N which is the number of samples and must be an integer, T_p and f_p are time and frequency of the desired signal, T_{master} is the period of the master clock and f_{master}= 16MHz is the master clock frequency. Considered that the time displacement of the sine signal (T_p) equals 2.5 msec (single bit time), where M equals 10, then the number of samples equals 250 samples.
A binary data signal $s(t)$ is used to control a ramp generator whose action is to create a ramp signal a ccording to the value of $s(t)$ at any given instant t. This ramp signal has been used in driving VCO to get the linear frequency modification signal of positive or negative inclination, in

accordance with the nature of input signal (which are the signals in which transition between amplitude levels occur under fixed rates). To achieve this purpose, a couple of integration block was used, in which the time constant controls the block output pulse width. A narrow pulse (Strobe signal) acts on reducing the output amplitude to zero within a limited time period, and then the integration unit starts its action again. To achieve that, the analog circuit available in the integration block has been used, whereas a set of collection units was used to form the signals in order to get the final form of the Ramp signal as shown in Fig. 4. (FPAA1&2), which is illustrated on a programmable signal writer as shown in Fig.5; whereas Fig.6 shows the lab results of the generator output. Output of this mass represents a linear frequency modification signal, with positive or negative inclination that corresponds with the input data nature. In other words, this block acts as the VCO, as it transforms the single sided Ramp signal to a sine signal with variable frequency the value of which corresponds with the variable value in this signal amplitude, as illustrated in Fig. 7.

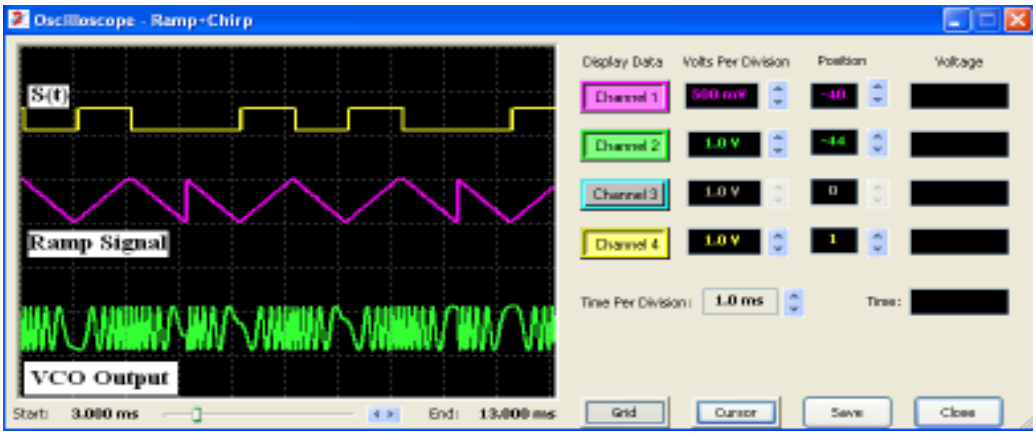

Fig.5 The programmable signal writer output.

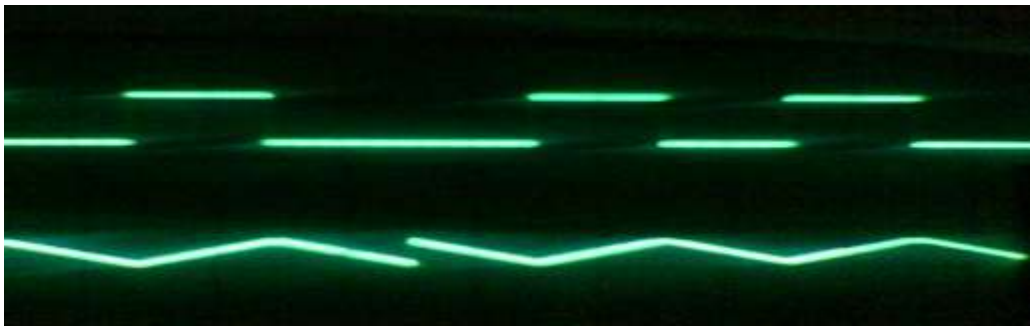

Fig.6 The lab results of the generator output.

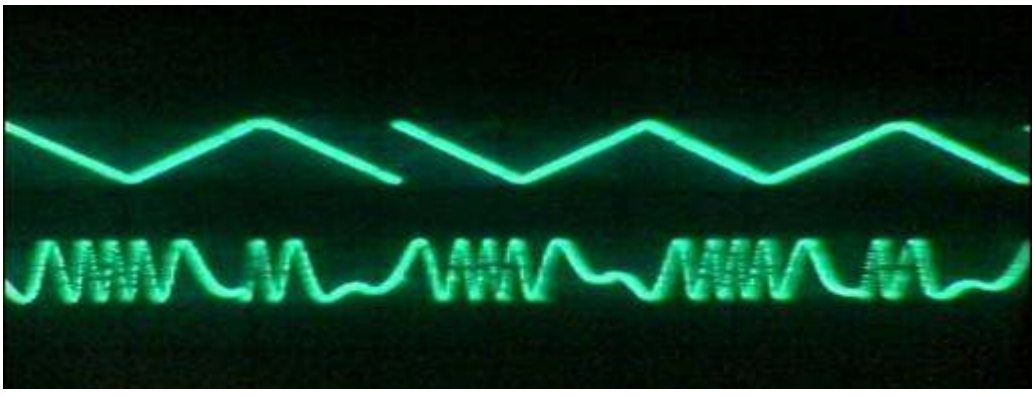

Fig.7 The VCO circuit output

Conclusions:

The field programmable analog arrays offer multiple advantages that exceed the advantages offered by the other electronic components, in reducing the time taken in designing the different analog circuits; in addition to the possibility of reforming the different circuits for the purpose of getting a design of high reliability. The research discusses the design and performance of an advanced VCO to be used in the field programmable analog arrays, as discussed in previous section. A programmed pattern of the circuit proposed in the research has been placed, in addition to exposition of its input and output signals. The measurements which got gave an indication of the proposed circuit competency and reliability. The single-sided Ramp signal of positive or negative inclination has been used in the VCO circuit drive, through amplitude to form the linear frequency modification signal. The proposed circuit is distinguished for its high stability, low power consumption, in addition to limited noise effect.

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