# LOOK TO SIMULATION OF FIRST ORDER PCM MULTIPLEXER [+]

**Sabbar Nusseif Jasim** [*] **Uzba haiyeed Selman** *

**Abstract:**

**This research deals with a look to the process simulation system of first order PCM(pulse code modulation) multiplexer has been achieved by designing the system on the basis of implementing its functions using simple logic for the logic circuits (logic gates) .**

**That the perception of the process simulation of the system had been considered in accordance with the rules of the International Union to meet the basic requirements of standardization (*ITU-T*) Rec. G.703, G704, G706, G732 and G823 related to line coding and pulse shaping, frame structure types (FAS, CRC-4, CAS and CCS), modified *Communication* Research Centre CRC-4 multiframe, errors detection and jitter tolerance respectively, are simulated.**

**Keywords:** **PCM,TDM,ITU-T,FAS,CRC,CAS,CCS,HDB3,TS0, RAI, BDH, LOF, AIS**

## محاكاة منظومة المستوى الاول للمازج الرقمي

صبار نصيف جاسم عزبه حميد سلمان

**المستخلص:**

يتناول هذا البحث نظرة الى عملية محاكاة منظومة المستوى الأول للمازج الرقمي وأن بناء هذه المنظومة تم عن طريق تشكيل وظائفه باستخدام المكونات المنطقية البسيطة للدوائر المنطقية (البوابات المنطقية) .

أن النظرة الى عملية المحاكاة للمنظومة قد بحثت وفق قواعد الاتحاد الدولي للاتصالات وضمن التوصيات الموجودة في المواصفات G.703, G704, G706, G732 and G823 المتعلقة بشكل وتشفير البيانات وتركيب أنواع الصيغ (FAS,CRC-4 ,CAS,CCS) وتعديل الصيغة المتعددة CRC-4 وكشف الأخطاء والتفاوت المسموح لل Jitter على التعاقب.

## Introductiond :

Pulse code modulation (PCM) is a communication technique with 50-plus-years history. PCM applies two basic concepts: time devision multiplexing (TDM) and amplitude quantization. The first order PCM multiplexer for the European standard system " E1" is one of the telecommunication transmission types of equipment that used the technique of TDM (time division multiplexer) . The " E1 " multiplexes 30 voice channels through TDM using 8000 samples per second per channels, and an 8-bit word for coding, and their signaling information rate is 2.048 Mb/s at one direction, and demultiplexes a 2.048 Mb/s digital signal into 30 channels of analog voice signals at the opposite direction.

The E1 Framer Core contains all the necessary functions and signals with the combination of an E1 Line Interface Unit (LIU) to provide a complete E1 data solution. Recovered signals from the LIU are fed into the High-Density-Bipolar three (HDB3) decoder and converted to a

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[*] **Technical Institut / AL-Dor**

Non-return-to-zero (NRZ) serial stream before being sent onto the receive framer for processing.

The received framer locates the frame and multiframe boundaries and monitors the data stream for alarms and errors. The frame buffer and slip modules allow the user to implement independent clocking between the network and backplane system. The transmitted framer processes the data stream and can be configured to insert both frame and Multiframe information.

## Frame Formats:

The basic E1 frame consists of 256 bits, beginning with 8 overhead bits, followed by 248 payload bits. The overhead bits or the first timeslot (timeslot zero, TS0) is reserved for framing, error checking and alarm signals, and the payload bits is divided into 31 channels (timeslots), consisting of 8 bits per channel. The individual channels can be used for 64 Kb/s PCM. Sometimes a timeslot (such as TS16) is reserved for signaling data (channel associated ABCD signaling). The bit rate for the E1 frame is fixed at 2.048 Mb/s. [1]

This basic frame format is combined into various multiframe formats as defined in ITU-T Rec. G.704 the Frame Alignment Signal (FAS)/Not FAS (NFAS), CRC-4 multiframe, and CAS multiframe structures described in the following sections.

## FAS/NFAS Framing

Two distinct basic frame types are defined, one with the Frame Alignment Signal (FAS) word in Time Slot 0 (TS0), and one with the Not FAS (NFAS) word in TS0. These two different frame types are alternately transmitted, and are used to determine frame synchronization, and provide bandwidth for maintenance and overhead functions. The bits of TS0 have specific definitions, and Table 1 shows the entire doubleframe structure.[ 1,2]

**Table 1 The E1 Timeslot 0 (TS0) Bit Allocation.**

| | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 8 |
|---|---|---|---|---|---|---|---|---|
| FAS | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| NFAS | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |

The function of each bit in Table 2-1 is described below:

a.The Si bits are reserved for international use and when unused are set to logic 1.
b. Bit 2 of the NFAS frames is fixed to “1”.
c.Bit 3 of the NFAS is the remote alarm indication RAI (A bit) for sending an alarm to the far end.
d. Bits 4-8 of the NFAS (Sa4-Sa8) whose use may be as follows:
- i-Bits Sa4 to Sa8 may be used in specific point-to-point applications.
- ii-Bit Sa4 may be used as a message-based data link application.
- iii-Bits Sa5 to Sa7 are for national usage.
- iv-Bits Sa4 to Sa8 may be used in Plesiochronous Digital Hierarchy PDH synchronization states messages.

Bits Sa4 to Sa8 (where these are not used) should be set to “1".

Once the demultiplexer has achieved frame alignment, it can separate the individual 64 Kb/s channels in the frame. If three frame alignment words in four are received in error, the terminal declares loss of frame alignment and initiates a resynchronization process. The recovery criteria is one correct frame alignment word, one non-frame word bit 2 (logic1), followed by one correct frame alignment word.

Loss of Frame Detection

• Loss of FAS/NFAS frame synchronization may be caused by several events. They include:
• Loss of signal (but not coupled to Loss Of Frame (LOF) detector/indicator).
• Continuous Reception of Alarm Indication Signal (AIS) (but not coupled to LOF detector/indicator).
• Three or more consecutive FAS words that contain single or multiple bit errors.
• Three or more consecutive NFAS words with bit 2 = 0 -or- three or more consecutive FAS words that contain single or multiple bit errors.

## CRC-4 Multiframe Structure

The new CRC-4 frame structure is defined in ITU-T Rec. G.704. The CRC-4 remainder is calculated on complete blocks of data including all payload bits, and the 4-bit remainder is transmitted to the far-end for comparison with the recalculated CRC-4 remainder. If the two 4-bit words differ, then the receiving equipment knows that one or more errors are present in the payload. Every bit is checked so an accurate estimate of block error rate (or errored seconds) is made while the link is in-service.[ 3]

The CRC-4 framing algorithm is more complex and is extremely unlikely to be fooled by payload data patterns.

Another powerful feature of CRC-4 framing provides a local indication of alarms and errors detected at the remote end. When an errored SMF is detected at the remote end, one of the E-bits is changed from 1 to 0 in the return path multiframe. The local end therefore has exactly the same block error information as the far-end CRC-4 checker. Counting E-bit changes is equivalent to counting CRC-4 block errors. In the same way, the A-bits return alarm signals for loss of frame or loss of signal from the remote end.[ 3,4]

## CAS Multiframe

Once the multiplexer has gained frame alignment, it searches in TS16 for the multiframe alignment signal (0000) in bits 1 to 4. This marks frame 0 of the group of 16 frames called the multiframe. The multiframe is only necessary when channel associated signaling (CAS) is used. Timeslot 16 then contains pairs of 4-bit ABCD signaling words. Over a complete multiframe all 30 channels are serviced. Table 2 below illustrates how sixteen state words are imbedded in TS16. [2,4]

**Table 2 Time Slot 16 Channel Associated Signaling Multiframe Structure**

| Frame No. | Time slot 16 Bit No. | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0 | 0 | 0 | 0 | 0 | X | Y | X | X |
| 1 | A1 | B1 | C1 | D1 | A16 | B16 | C16 | D16 |
| 2 | A2 | B2 | C2 | D2 | A17 | B17 | C17 | D17 |
| 3 | A3 | B3 | C3 | D3 | A18 | B18 | C18 | D18 |
| 4 | A4 | B4 | C4 | D4 | A19 | B19 | C19 | D19 |
| 5 | A5 | B5 | C5 | D5 | A20 | B20 | C20 | D20 |
| 6 | A6 | B6 | C6 | D6 | A21 | B21 | C21 | D21 |
| 7 | A7 | B7 | C7 | D7 | A22 | B22 | C22 | D22 |
| 8 | A8 | B8 | C8 | D8 | A23 | B23 | C23 | D23 |
| 9 | A9 | B9 | C9 | D9 | A24 | B24 | C24 | D24 |
| 10 | A10 | B10 | C10 | D10 | A25 | B25 | C25 | D25 |
| 11 | A11 | B11 | C11 | D11 | A26 | B26 | C26 | D26 |
| 12 | A12 | B12 | C12 | D12 | A27 | B27 | C27 | D27 |
| 13 | A13 | B13 | C13 | D13 | A28 | B28 | C28 | D28 |
| 14 | A14 | B14 | C14 | D14 | A29 | B29 | C29 | D29 |
| 15 | A15 | B15 | C15 | D15 | A30 | B30 | C30 | D30 |

Notes:
Frame 0 bits 1- 4 define the time slot 16-Multiframe alignment.
X = time slot 16 spare bits.
Y = yellow alarm or time slot 16 remote multiframe alarm (RMA) bit (1 = alarm condition).

**Simultaneous CAS and CRC-4 Multiframe**

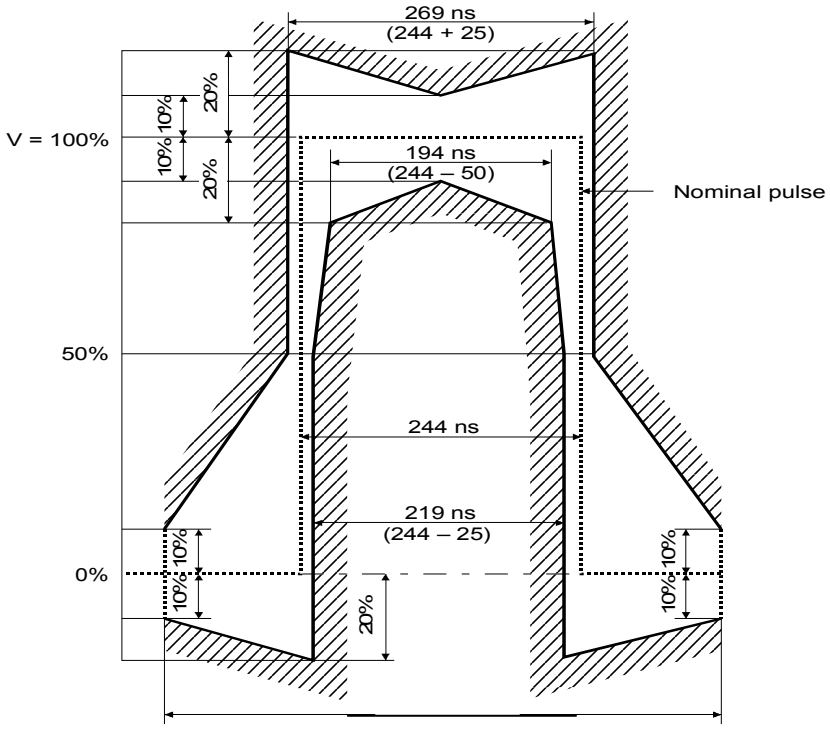
This mode of framing is identical to CAS Multiframing except that TS0 is defined by the CRC-4 Multiframe structure rather than the FAS/NFAS Doubleframe structure. The CAS multiframes are not necessarily synchronized to the CRC-4 multiframes. This mode is enabled simply by simultaneously enabling CAS and CRC-4 multiframing.[ 5]

**Line coding:**

Two types of line coding are used in a typical E1 2.048 Mb/s network:
Alternate Mark Inversion (AMI) and High Density Bipolar 3 (HDB3). HDB3 is the coding used most commonly for 2M, 8M, and 34M. The clock recovery circuits of the receivers can operate well, even though the data contains long strings of zeros.

**PULSE SHAPING[4,7] :**

The template for the transmitted pulse, as specified in ITU-T Rec. G.703, is shown in Figure-1. The ratio of the amplitude of the transmit pulses generated between two levels.




488ns
244+244

**Figure 1 The pulse shape at 2.048 Mb/s interface**

**Simulation of first order pcm multiplexer:**

A block diagram of the first order PCM multiplexer is shown in Figure 2. It consists of three major sections: transmitter, receiver and slip buffer. The transmitter section comprises of the 32 lines multiplexer, E1 counter, loop back and idle word insertion unit, the framing and CRC-4 coding insertion unit, the HDB3 encoder, and the pulse shaping unit. The receiver

is comprised of the regenerative unit, the HDB3 decoder and the framer, which recovers synchronization and detects alarms and errors.

For Transmit side, the transmitted serial data come from 32 lines multiplexer, the signaling bits can come from the transmit signaling 32 lines multiplexer and all timing signals from clock are applied to transmitter side. PCM idle code loopback insertions are performed under loopback unit. TS0 insertion data includes the FAS/NFAS frame synchronizing pattern, CRC-4 information and various reserved bits. TS16 insertion functions include the CAS signaling multiframe alignment pattern and transmit signaling bits. All framing and internal data insertion can be enabled to the multiplexer transmit data stream.[ 1,3,5]

The composite serial data is then routed to the HDB3 encoder who performs zero-code suppression as well as conversion to a bipolar data stream. The transmit line driver then interfaces this signal to the physical E1 line via an external transformer, compatible with 120 Ω cables. [8]

The received bipolar input data can be obtained from the regenerative unit. The regenerative unit uses adaptive decision levels to allow for up to 18 dB of cable loss and the timing recovery unit which consists mainly of a Digital Phase Locked Loop (DPLL). After clock and data have been recovered, HDB3 decoding is performed to remove zero-code suppression and to convert the bipolar data into a single unipolar data stream. The resulting serial data is then checked by the framer for the G.704 frame Alignment Signal (FAS), the G.706 CRC-4 multiframe, and the G.732 Channel Associated Signaling (CAS) multiframe. Data in channel 16 is routed to the received TS16 buffer circuit access to CAS bits. Data in each received time slot is read by either the slip buffer, or returned to the transmitter (per-channel loopbacks). Two complete frames of received data, including channel 0 and channel 16, are kept in the buffer memory.

The slip buffer reads the appropriate data from HDB3 decoding circuit and assembles the serial output stream at 32-line demultiplexer. Signaling freeze is also performed here, again by redirecting buffer read operations (and disabling receive data write operations).

*Timing system*

The E1 bus is a synchronous time division multiplexed serial bus with data streams operating at 2.048 Mb/s and configured as 32, 64 Kb/s channels. The system clock frequency is 2.048 MHz for all transmit side inputs and the output of the slip buffer at receiver side. Synchronization of the data transfer is provided from a frame pulse, which identifies the frame boundaries and repeats at an 8 kHz rate.[ 5,7]

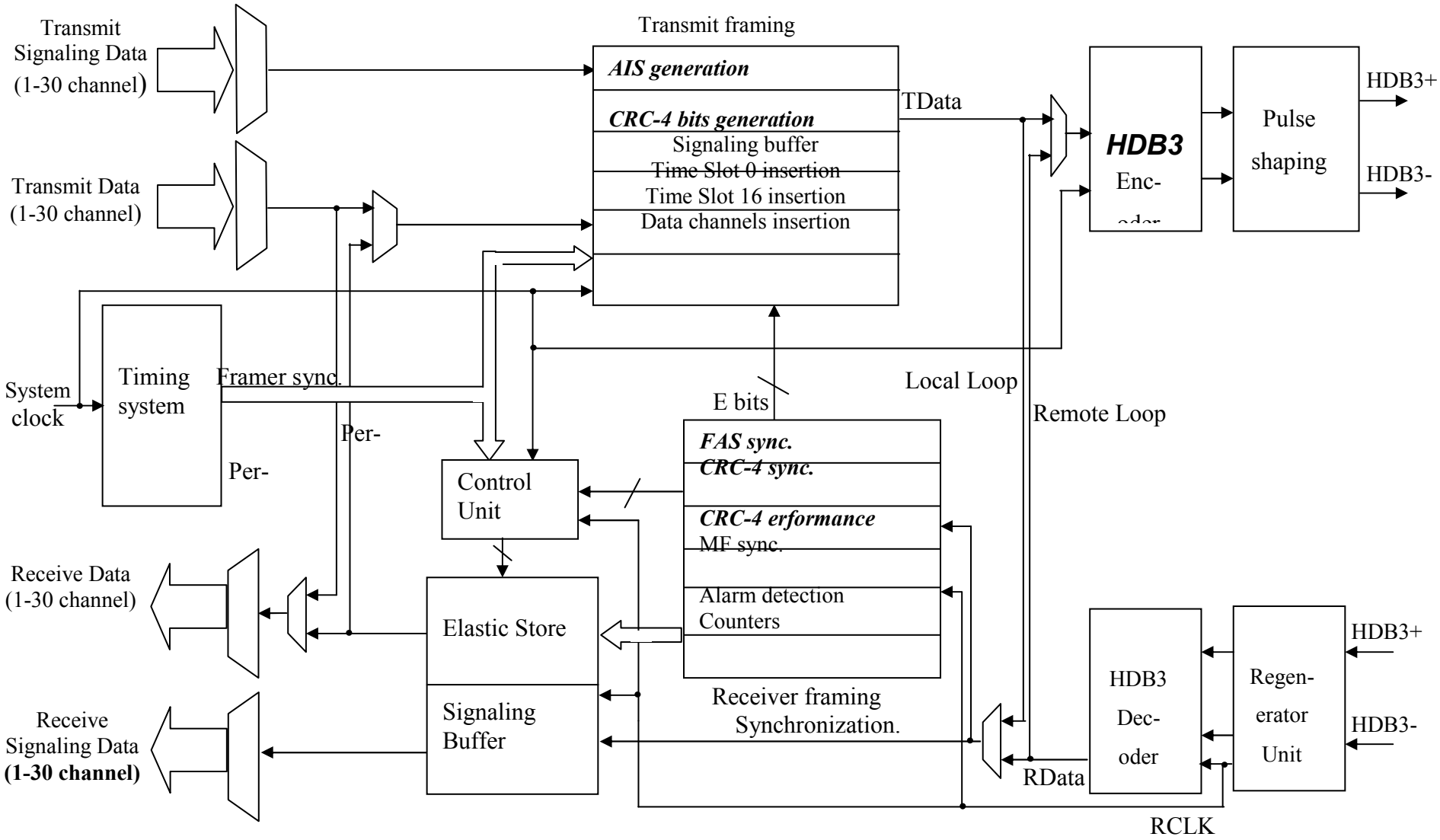



**Figure 2 Block diagram of first order PCM multiplexer**

## Transmit framing

The transmitted inputs for the system PCM bus interface consists of the unipolar transmit input signal, clock, and synchronization. Inserting the channel 0 and the channel 16 to the data stream generates the transmitted framing. A block diagram of the transmitted framing insertion is shown in Figure 3.

Two framing functions are provided in the transmitted data stream at TS0: a FAS framer and an NFAS framer. The transmit overhead generation circuitry provides the ability to insert all of the overhead associated with the primary rate channel while Alignment multiframe patterns and Remote Multiframe Alarm (RMA) inserted in TS16.[ 2]

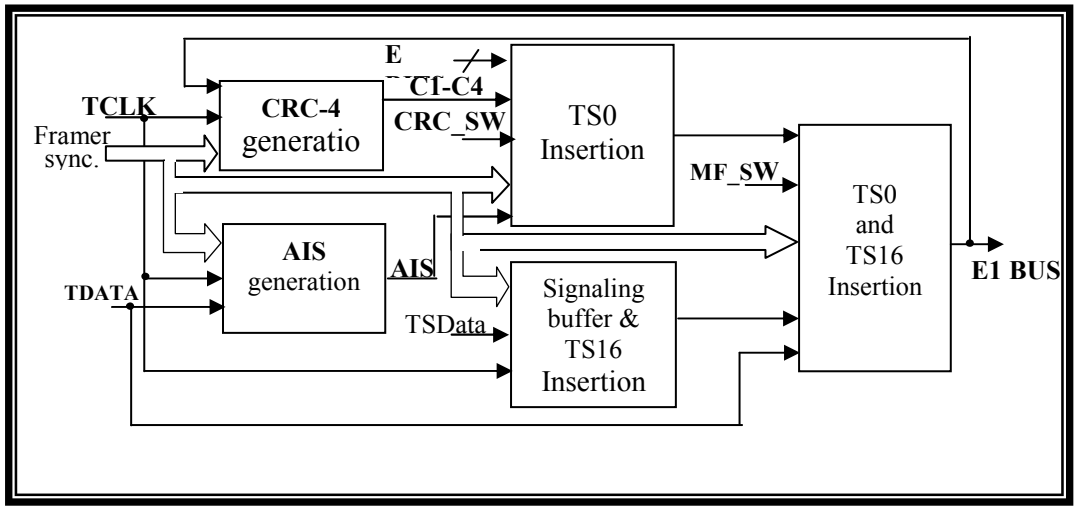



**Figure 3 Block diagram of the transmit framing.**

## CRC-4 bits generation

The CRC-4 frame alignment verification functions as follows. Initially, the CRC-4 operation must be activated and CRC-4 multiframe alignment must be achieved at both ends of the link. All the bits of every transmitted submultiframe are passed through a CRC-4 Generator polynomial of the shift register (x4 + x + 1) as shown in Figure 4.

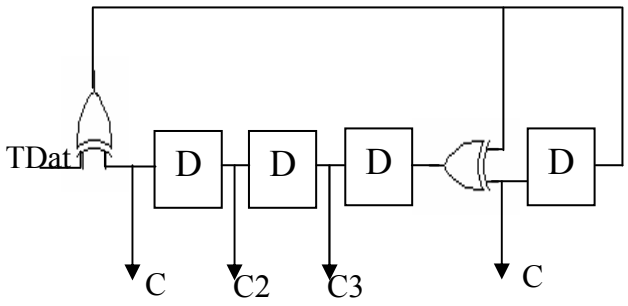



**Figure 4 The CRC-4 Generator polynomial circuit.**

Time slot 0 (TS0) insertion

The frame alignment signal (FAS) automatically insert data of the FAS word synchronizing pattern “0011011” in TS0 of the FAS frame. The bit “2” set to “1”, the Sa-bits

is set to "1" because they are not used and the A-bit insertion comes from AIS generation circuit and put in bit 3 in TS0 of the NFAS frame. [5]

For FAS/NFAS frame, bit number "1" is set to "1". If CRC-4 error checking and framing is desired, it must be enabled by setting the CRC-4 bits in bit number "1" of TS0 of the16-frame or multiframe. The bit "1" comes from CRC-4 bits generation circuit in TS0 of the FAS frame. If NFAS frame, the bit "1" in TS0 used to insert data of the MFAS word synchronizing pattern "001011" (in frames 1,3,5,7,9 and 11) and two spare bits (in frames 13 and 15), which are used for CRC-4 error performance reporting comes from the receiver.[ 6]

**Signaling Buffer**

The two 16-register Transmit Signaling Buffer stores a single multiframe of signaling data input from the 32 lines signaling multiplexer for insertion into TS16 and updated of each multiframe. Each register in the buffer is organized into a Time Slot n and a Time Slot n+16-signaling sample (4 signaling bits or nibbles for each channel).

Time Slot 16 (TS16) insertion

The Signaling bits for each channel are grouped as 4-bit nibbles. Two signaling nibbles for a pair of PCM channels are required to be inserted in TS16 of the 1-15 frames. For frame 0 specified CAS multiframe alignment pattern "0000" is inserted in the higher order quartet of channel 16, while the lower order quartet of channel 16, the X bits and RMA bit is inserted. The X bits set to "1" because it is not used. If CCS framing is desired, then channel 31 is inserted into TS16.

The data output from the TS0 and TS16 insertion blocks are multiplexed together with channels data (time slots 1-15 and 17-31). Random data is inserted stream data before starting transmitting actual data to reduce the time required for synchronization at the receive side. The HDB3 transmitter encodes an NRZ binary unipolar input signal and a synchronous transmission clock from transmit framing insertion into two HDB3 binary bipolar output signals (+HDB3, -HDB3).[6,8]

**Pulse Shaping**

A method of pulse shaping is to generate the waveform directly, using a transversal filter (tapped delay line). The data input to the pulse generator comes from HDB3 encoding and transfers output signal at the physical E1 lines.

Receiver line interfacing circuit

The Receive line interfacing circuit or regeneration circuit recovers clock and data from the bipolar HDB3 line signal that has been attenuated and distorted due to the characteristics of the line. The block diagram of the regenerated circuit as shown in Figure 5. The receiver portion of the regeneration circuit consists of a smoothing filter, an optional two-stage equalizer, peak detector, data slicer and a clock extractor.

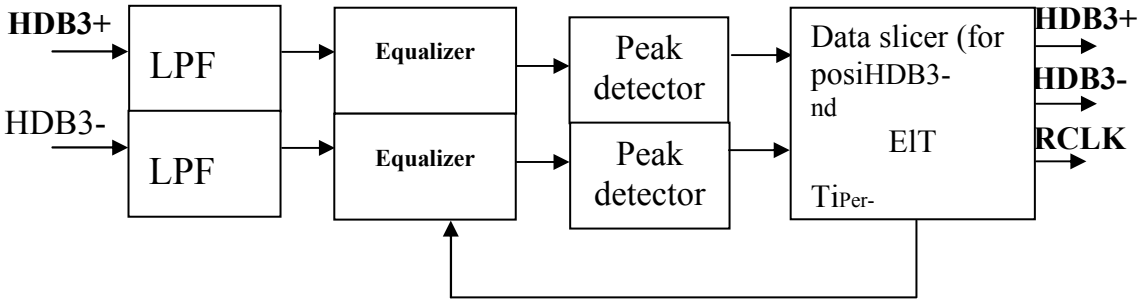



**Figure 5 Block diagram of the regenerate circuit.**

**HDB3 Decoding**

The receiver decoder converts two HDB3 binary bipolar inputs (+HDB3, -HDB3) with clock synchronization from regenerated circuit into unipolar signal NRZ. The simulated circuit, which performs the HDB3 reception decoding, functions with error detection and correction.[ 2]

The simulation circuits removes from bipolar input after error correction the extra 'marks' of the same polarity and then converts into unipolar signal NRZ. This requires three pulses delay time and performed in two steps:

1-Converts HDB3 data input positive and negative to decoded HDB3 positive and negative.

2-Decode HDB3 positive and negative to remove extra 'marks' violations and to converts to NRZ unipolar signal.

**Receiver framing synchronization**

The receiver framing synchronization input clock and data recovery from HDB3 decoder and outputs recovered frame synchronization. [4,9]

There are three distinct framers within the multiplexer system. These include a frame alignment signal framer, a multiframe framer and a CRC-4 framer. Figure 6 shows the state diagram of the framing algorithms.

In the beginning receiver, the FAS framer synchronization enabled to searches for the first FAS framer within the bit stream. Once detected, the frame counters are set to find the non-frame alignment signal. If bit 2 of the NFAS is not one, a new search is initiated; else the framer will monitor for the frame alignment in the next frame. If the FAS framer is found, the device immediately declares frame synchronization (channel clock, frame clock and multiframe clock).

The CRC-4 multiframe enabled when selects CRC-4 multiframe and found FAS framer. Once frame alignment synchronization is acquired, the CRC framer must find two framing signals in bit 1 of the non-frame alignment signal. Upon detection of the second CRC framing signal the simulation circuit will immediately go into CRC synchronization. When maintenance feature is enabled the CRC framer will force a complete reframe of the device if CRC frame synchronization is not found within 8 ms or more than 914 CRC errors occur per second.

The multiframe synchronization algorithm is also dependent upon the state of FAS framer. The MF enabled when selects MF framer or is established when state of CRC-4-to-NCRC-4 equipment. The multiframe framer will not initiate a search for multiframe synchronization until frame synchronization is achieved. Multiframe synchronization will be declared on the first occurrence of four consecutive zeros in the higher order quartet of channel 16. Once multiframe synchronization is achieved, the framer will only go out of synchronization after detection of two errors in the multiframe signal or loss of frame alignment synchronization.

**Alarm indication [ 7]:**

1-If AIS set to "1" for three consecutive FAS framing, the blue alarm set to "1" and not return to "0" before receiving three consecutive "0" of AIS alarm.

2-If AIS set to "1" for two consecutive CAS multiframing, the yellow alarm set to "1" and not return to "0" before receiving two consecutive "0" of AIS multiframe alarm.

3-If the framing algorithm is not found through 2.5 second the system indicate long time synchronization and Red Alarm set to "1".

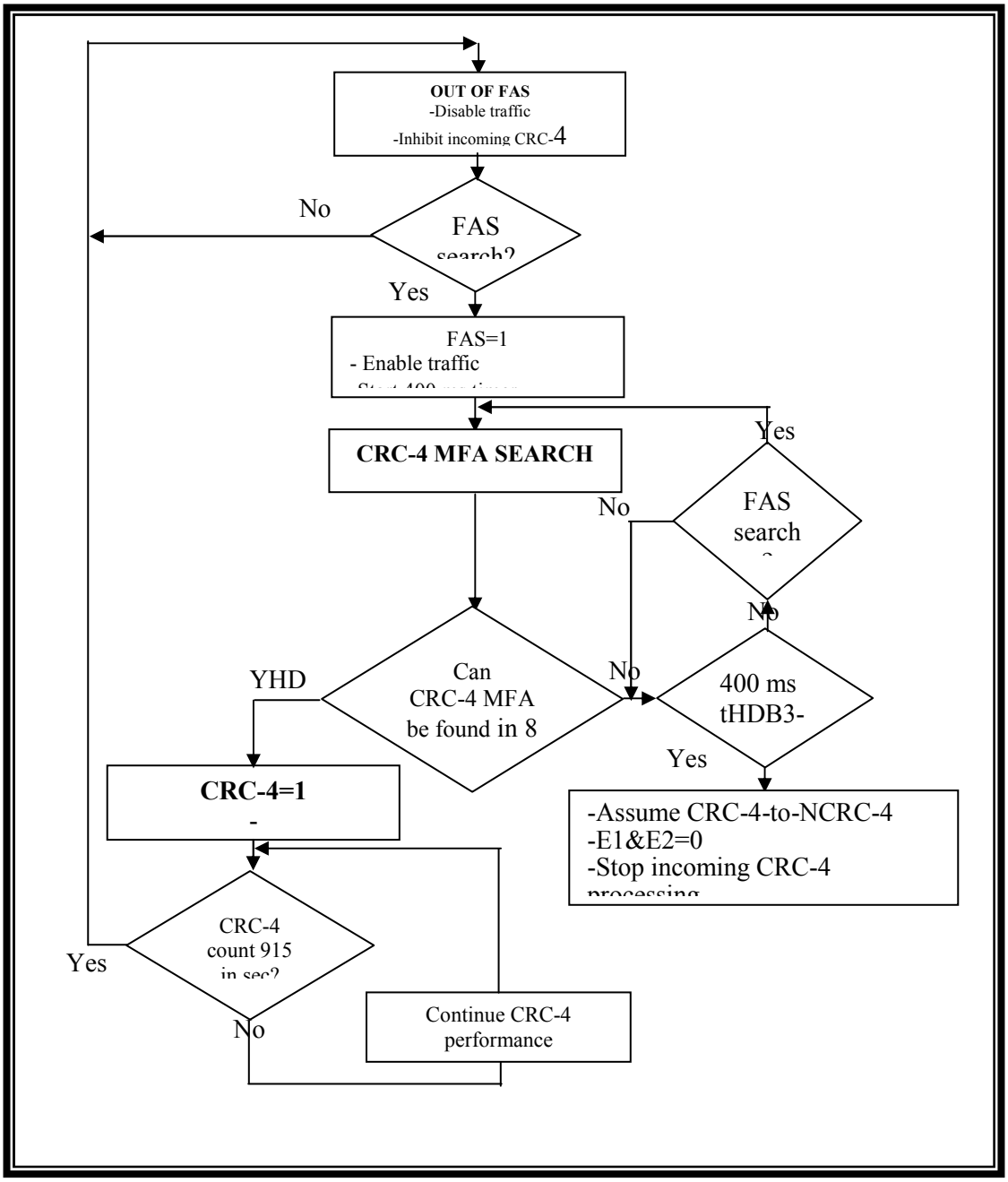



**Figure 6 Framing algorithm**

**For the following consequent actions are taken[1,3]:**

1- Manual re-framing of the received FAS framer and signaling multiframe alignment functions can be performed at any time.
2- The FAS framer, signaling multiframe alignment, and CRC-4 multiframe alignment functions operate in parallel and are independent.
3- The receive channel associated signaling bits and signaling multiframe alignment bit will be frozen when multiframe alignment is lost.
4- The transmit RAI bit will be one until FAS framer is established, then it will be zero.
5- E-bits can be optionally set to zero until the equipment interworking relationship is established. When this has been determined one of the following will take place:
a-CRC-4-to-NCRC-4 operation - E-bits = 0.

b- CRC-4-to-CRC-4 operation - E-bits as per G.704 .

6- All manuals reframe and new FAS framer searches start after the current frame alignment signal position.

7- After FAS framer has been achieved, loss of frame alignment will occur any time three consecutive incorrect FAS framer signals are received. Loss of FAS framer will reset the complete framing algorithm.[ 1]

8- When CRC-4 multiframing has been achieved, the primary FAS framer and resulting multiframe alignment will be adjusted to the FAS framer determined during CRC-4 synchronization. Therefore, the primary FAS framer will not be updatedduring the CRC-4 multiframing search, but will be updated when the CRC-4 multiframing search is complete.

**Elastic Store and signaling buffer**

To enable received signal synchronization to a single clock reference, the received circuitry provides elastic store and signaling reinsertion. The elastic store removes all input jitter because elastic store outputs are synchronized to the local system clock.

The elastic store reads the appropriate data from HDB3 decoding circuit and assembles the serial output stream at 32-line demultiplexer insertion, while frame synchronization reads from receiver framing to enabled elastic store and signaling buffer. The recovered serial data, the slip buffers data and slip multiframe synchronization signals are provided to the user.[ 5]

Idle code insertion and loopback functions can be performed only on the elastic store output. (The receive per-channel controls actually refer to the elastic store) Controlled frame slips are performed when the elastic store skips or repeats a frame (256 bits). Signaling freeze is also performed here, again by redirecting buffer read operations (and disabling receive data write operations). The slip buffer synchronization output is multiframe synchronization, and transitions high-to-low at the beginning of TS0, frame 0 of the 16-frame multiframe. This synchronization output is compatible with the transmit synchronization input, which allows the direct connection of the elastic store output to transmit input.

**Loopbacks**

The provided four loopback modes are local, remote, local per-channel and local per-channel line loopbacks.

**- Remote Loopback**

Remote loopback for a framer is enabled when a remote switch set to “1”. Remote loopback connects the received line data back to the transmitter.

**- Local Loopback**

Local loopback for a framer is enabled when a local switch set to “1”. Local loopback connects the transmit path with the receive path in the direction toward the line.

**-Remote Per-Channel Loopbacks**

The Remote Per-Channel Loopbacks for time slot is enabled when TSnr switch is set to “1”. Single time-slot line loopback connects the receive line data back to the transmitter, as the remote loopback but the switch is for each channel using 32 multiplexer. The loopback is performed before the 32-line demultiplexer.

**-Local Per-Channel Loopback**

The Local Per-Channel loopback for time slot is enable when TSnl switches set to "1". Single time-slot line loopback connects the transmit path with the receive path in the direction toward the line, as it the local loopback but the switch for each cannel by using 32 multiplexer. The loopback is performed after the 32-line multiplexer.

## Conclusions:

A design for E1 multiplexer bus based one implementing ITU_T related recommendations G.703, G.704, G.706, G.732 and G.823 has been made.

A simulation of E1 multiplexer bus design has been made using the Matlab Simulink. The results of simulation test showed successful implementation of bus functions.

Jitter effect reduction was made using DPLL and elastic store. The elastic store is very useful for solving the problem of frequency difference between the transmitted and receives clocks.

The transmit side frame is totally independent from the received side in both the clock requirement and characteristics.

Data channel loading on the transmitted E1 bus was done with the extra bits (DTS0 and DTS16) directly without any timing delay.

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