PC BASED POWER LINE FREQUENCY MONITORING AND ARCHIVING SYSTEM [+]

منظومة مراقبة وأرشفة تردد خط القدرة باستخدام الحاسبة الشخصية

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Abstract:

The work presented in this paper concerned with the design and implementation of the power line frequency monitoring and archiving system based on the personal computer. The frequency measuring board was implemented and the interfacing process with the personal computer via serial port was performed. In order to monitor the frequency readings a graphical user interface program has been implemented together with data archiving program. Experimental results show an accurate and reliable system.

المستخلص:

العمل المقدم في هذا البحث يتعلق بتصميم وتنفيذ نظام مراقبة وأرشفة باعتماد الحاسوب الشخصي. تم تنفيذ جهاز قياس التردد وتنفيذ ربطه باستخدام الممر التسلسلي للحاسوب الشخصي. لغرض مراقبه قراءات التردد تم تنفيذ برنامج المستخدم التفاعلي سويا مع برنامج الأرشفة. النتائج العملية أظهرت دقة ووثوقية النظام.

Introduction:

Frequency deviation is a common problem for power system signal processing. The actual frequency may deviate from the normal value from time to time due to various reasons such as disturbances and subsequent system transients [1]. Industrial power system applications require close monitoring of the deviations in supply frequency, because the frequency is very much dependent on the real power balance in power system network. Normally the rate of generation of energy must equal the rate of energy consumption plus losses. But small or large changes in load always take place in the system and the random nature of the load fluctuations renders it difficult to achieve a perfect match between input and load demand at every instant. This mismatch leads to system frequency fluctuations [2]. Accurate information of supply frequency variation is essential for satisfactory operation of interconnecting power systems.

Application Architecture:

The objective of the proposed system is a user with PC can read the frequency data from the frequency measurement unit and check the history of the measurement data by using the developed archiving system.
The architecture of the proposed application shown in Figure1.

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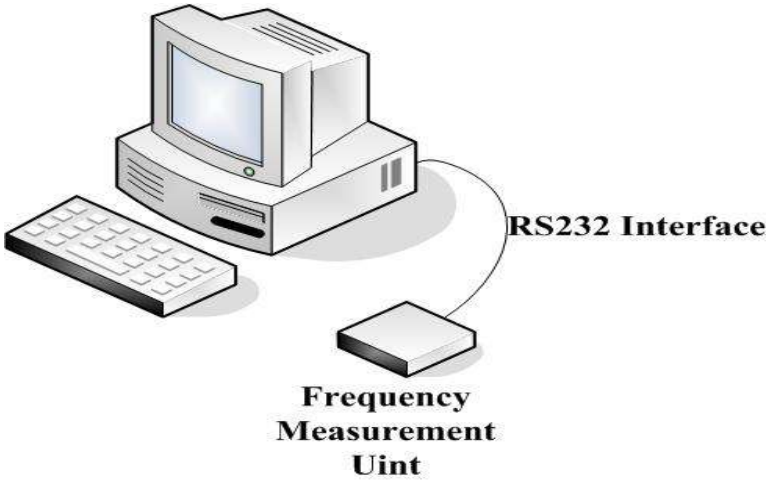

Figure 1. System Architecture

The functionality of the Monitoring and Archiving system is implemented by software modules written in visual basic studio 6.

Technological Requirements:

The following technology is used to realize the system architecture:

• PC to receive and visualize data with Windows XP operating system.
• Voltage Transformer, Square Wave Generator, Phase-locked loop (PLL), counters, NOR gates, UART, and MAX232.
• visual basic studio 6 quick language to create windows applications, High speed processing, Support RS232 Interfacing, and Visual Basic Generally fit applications databases.

Hardware design:

The block diagram of power line frequency measurement unit is shown in Figure 2.

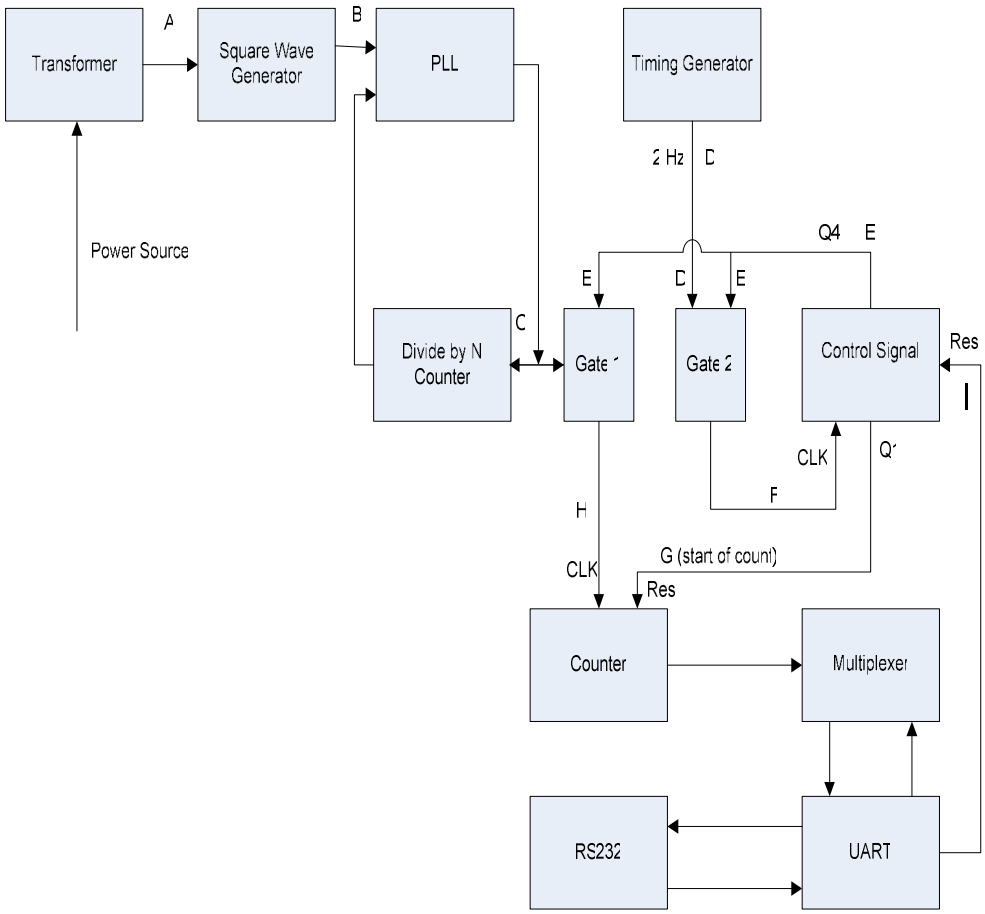

Figure 2. Frequency sensing unit

The transformer used in this design is a step down for the input voltage where the output of the transformer is fed directly to a square wave generator circuit. The sinusoidal signal output of the transformer must be convert into a form suitable for electronic circuits. 2N222 NPN transistor is designed for high-speed switching applications [3], is used to generate square wave.

Phase-locked loops (PLLs) have significantly increased use in signal-processing and digital systems. Frequency modulation (FM) demodulation, frequency shift keying (FSK) demodulation, tone decoding, frequency multiplication, signal conditioning, clock synchronization, and frequency synthesis are some of the many applications of a PLL. This architecture consists of three parts: phase comparator, low-pass filter (LPF), and voltage-controlled oscillator (VCO) connected to form a closed-loop frequency-feedback system [4]. PLL is actually implemented on single integrated circuit (type 4046) that consists of a low power, linear, voltage-controlled oscillator (VCO) and phase comparators [5].

The PLL in this application is used as frequency multiplier to increase the resolution of the input signal by two digits after the decimal point, therefore the input signal is multiplied by 100 (50Hz * 100 =5000 Hz). Hence, the value of N must be equal to 100. The dual BCD (Binary Coded Decimal) counter (type 4518) is used in this design, it contains two identical independent internally synchronous 4–stage counters [3], the output of the first counter is fed directly to clock input of the second counter.

Timing generator is simply a 14-stage binary ripple counter (type 4060) with 32768 Hz crystal where Q14 of the counter is used to provide 2 Hz signal (32768 Hz / 2^14 = 2 Hz) this signal is used as clock input to the control signal stage (Johnson counter) through gate 2.

To count the frequency output from the VCO, the frequency must be taken as samples in 1 second. Gate and control signal performs this mechanism. The Quad 2-Input NOR gates (type 4001) is used in this application. The control signal is generated by using Johnson counter (type 4022) which is a 4-stage Johnson counter with 8 decoded outputs and a carry-out bit. The decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle [3]. The clock input to Johnson counter is 2 Hz this mean that each decoded output remains high for 0.5 second. Q1 of Johnson counter is used as reset signal for the counter stage, then the counter stage will start counts for Q2 and Q3 (1 second). Finally Q4 is used to stop the counter from counting where the output of both gates is 0, therefore there is no clock input to both Johnson counter and counter stage.

A 7-stage ripple-carry binary counter (type 4024) is used in this hardware to count the pulses. The maximum count of this counter is 2^7=128 while the output of the VCO is 5000 Hz, therefore two 7-stage ripple-carry binary counter is used to extend the count range to 2^14 =16 kHz which covers the total range of counting. Timing diagram of power line frequency measurement unit is shown in Figure 3.

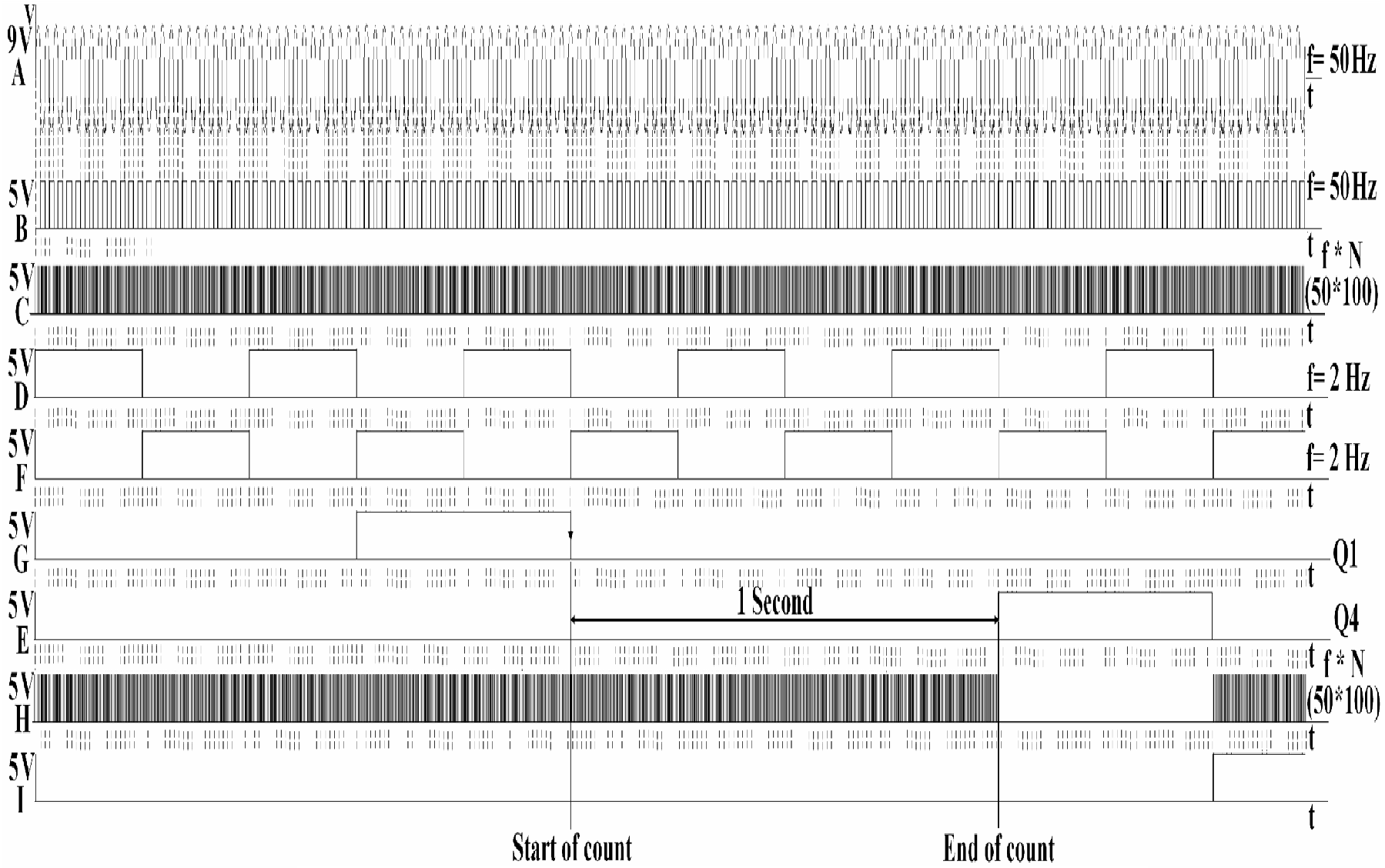

Figure 3. Timing diagram of the power line frequency sensing unit.

The 14 bits output of the two counters must be input to 8 bits of the UART to realize this one form of multiplexing is used. The quad AND-OR select gate (type 4019) is used for this purpose. Each one of them consisting of two 2-input AND gates driving a single 2-input OR gate [3]. This multiplexer has 8 bits input and 4 bits output, therefore two multiplexers are used and the 8 bits output of the multiplexers are connected to the 8 bits of the UART. The reading of the 14 bits will be done in two steps. The PC will read 8 bit (byte) in each step. Selection of byte is accomplished by control bits KA and KB of 4019.

The purpose of the UART is to receive a serial transmission and convert it into parallel data and vise versa. It prepares the received data for processing by converting the serial start, data, parity and stop bits into parallel form. The transmitting part converts parallel data into serial form and automatically adds start, parity and stop bits. The word length to be serially transmitted can be 5, 6, 7 or 8 bits with odd, even or no parity bit. The stop bit may be 1, 2 or 1.5 depending on the word length being transmitted. UART6402 is used for this application because it has a separate receive and transmit data buses, and the other reason is that the connecting pins to various logic levels can easily configure the UART. However, it requires an external baud rate generator, and its frequency should be 16 times faster than the baud rate of the serial transmission . Therefore, It is therefore necessary to generate a clock frequency for the communication and for this application the communication is set for 9600 baud (bits/sec) implying that the clock frequency must be 153.6 KHz (16x9600). The baud rate generating circuit consist of HCT4060 14-stage counter with 2.4576 MHz crystal oscillator. In this application the UART is configured for 8 data bits, 1 stop bit, and no parity checking [6].

The RS-232 is one of the most serial communications schemes in use is defined by the RS-232 family of standards. Most UARTs are designed specifically to support RS-232. RS-232 specifies that the least-significant bit of a byte is transmitted first and is framed by a single start bit and one or two stop bits. Common RS-232 data rates are known to many computer users. Standard bit rates are 2^N multiples of 300 bps. Logical transceiver level characteristics such as bit rate, error detection, and framing are accompanied by electrical transducer level characteristics, more commonly referred to as the physical layer of a communications link. RS-232 refers to the logic 1 state as a mark and assigns it a negative potential from –3 to –12 V. The logic 0 state is a space and is assigned a positive potential from +3 to +12 V. Since RS-232 inverts the logic levels, an idle link is held at negative voltage, logic 1. Serial communication is well suited to long distances, because fewer wires are used as compared to a parallel bus [7].

It is evident that the maximum RS-232 signal levels are far too high for computer logic, and the negative RS-232 voltage cannot be understood by all computer logic. Therefore, after receiving serial data from an RS-232 interface the voltage has to be reduced, and the low and high voltage levels inverted. Also when sending computer logic signals Transistor Transistor Logic (TTL) over the RS-232 the logic voltage has to be “pumped up”, and a negative voltage has to be generated too [6]. MAX232 chip which is a dual driver/receiver that includes a capacitive voltage generator to supply RS-232 voltage levels from a single 5 V supply [3], is used to carry out these voltage level conversions in this application. Figure 4 shows the circuit diagram of power line frequency measurement unit.

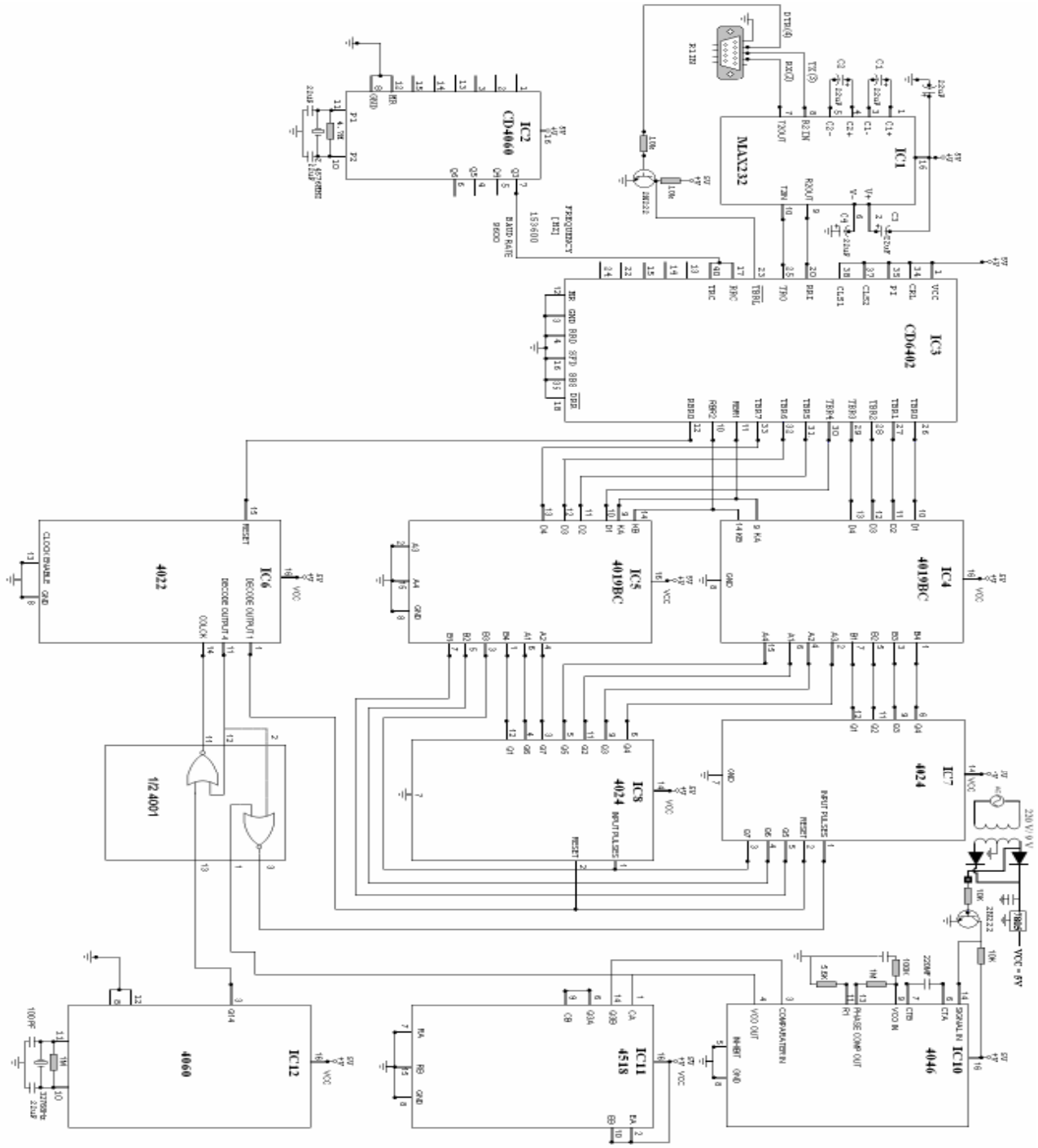

Figure 4. The circuit diagram of power line frequency measurement unit

A complete and functioning frequency measurement unit circuit is shown in Figure 5.

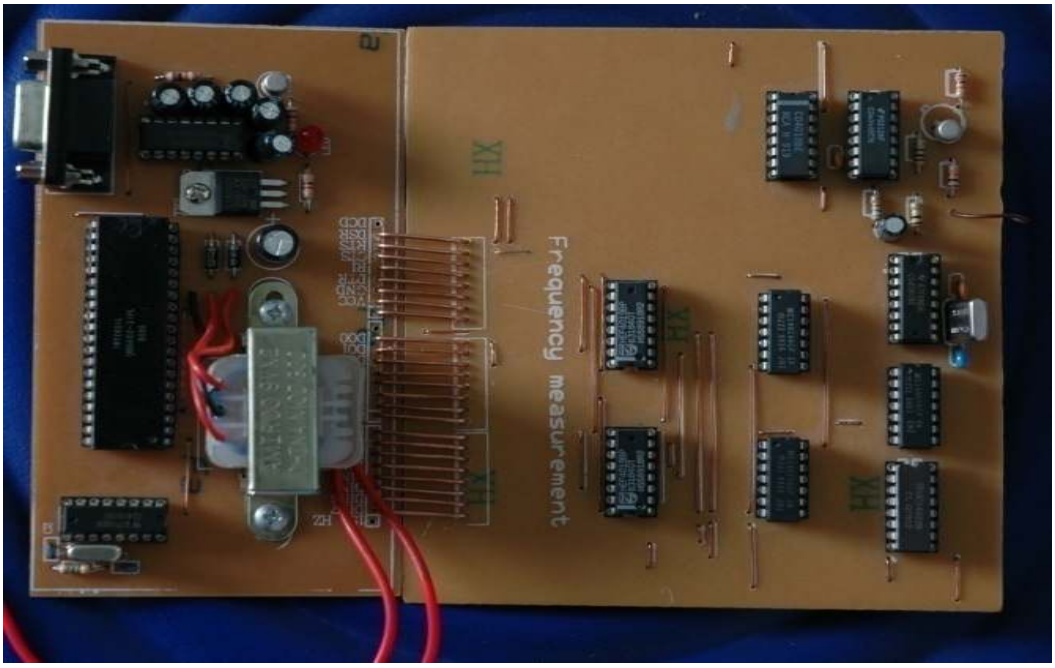

Figure 5. A complete and functioning frequency measurement unit

Software design

The software of the PC performs the following tasks:

- reading the data from frequency measurement unit
- processing the received data
- displaying results on screen
- putting the data in designed frequency history database

The flowchart in Figure 6 explains the program structure on which the PC depends to achieve the frequency data.

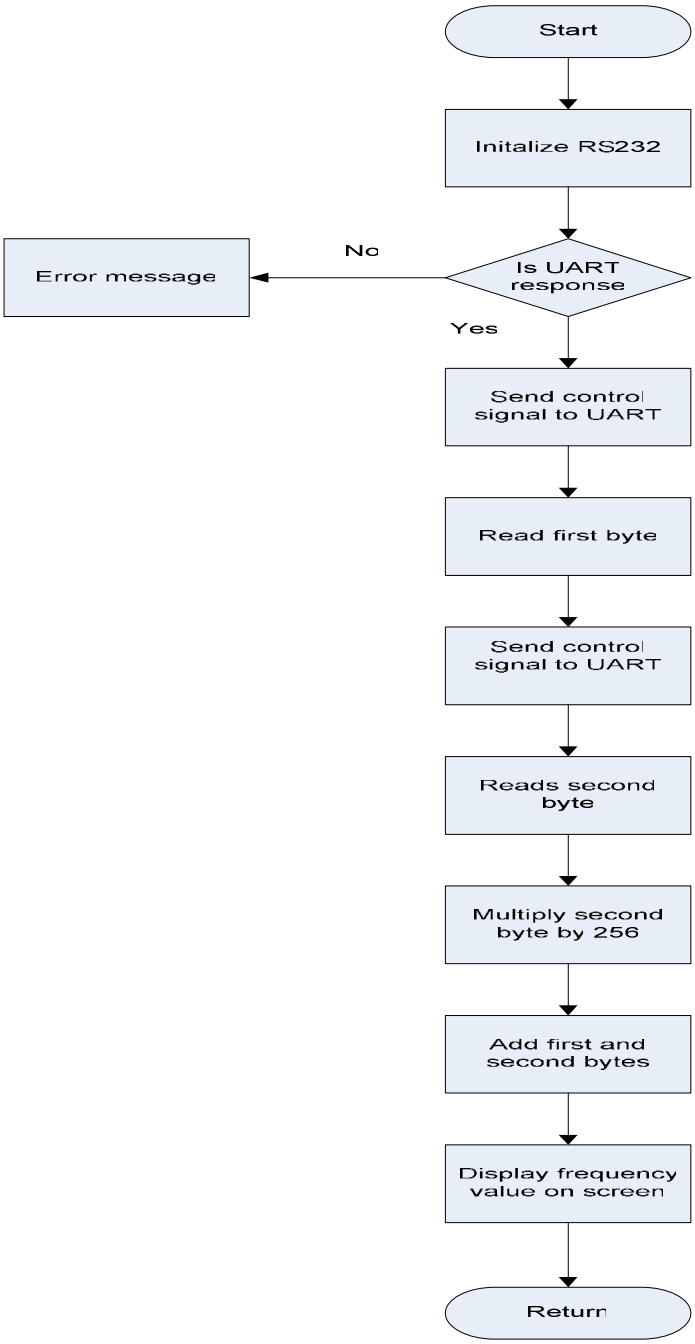

Figure 6. Frequency Reading Routine

Data visualization:

The application window displays the frequency as a digital clock with two digits resolution as shown in figure 7.

The frequency values are directly put in archiving system. The archiving system is 24 hour archiving system and there is separate database for every day. From which the user can read the value of the frequency at any given time or date. The user can show the frequency chart using frequency history command which causes to display the Reporting Program window as shown in figure 7. The user must input the date to check the readings of the power

line frequency at that day then just by click GO command the software performs the required action.

Figure 7. Application window of frequency monitoring.

Figure 8. Reporting Program Window

After short time a small window will appear as shown in Figure 9 that tells the user to see desktop. On desktop a file is created which show the frequency chart for the date entered. Figure 10 show the frequency chart of 30/6/2008.

Figure 9:Report Messag

The chart gives the frequency in range 48.50 to 50.50 during 24 hour.

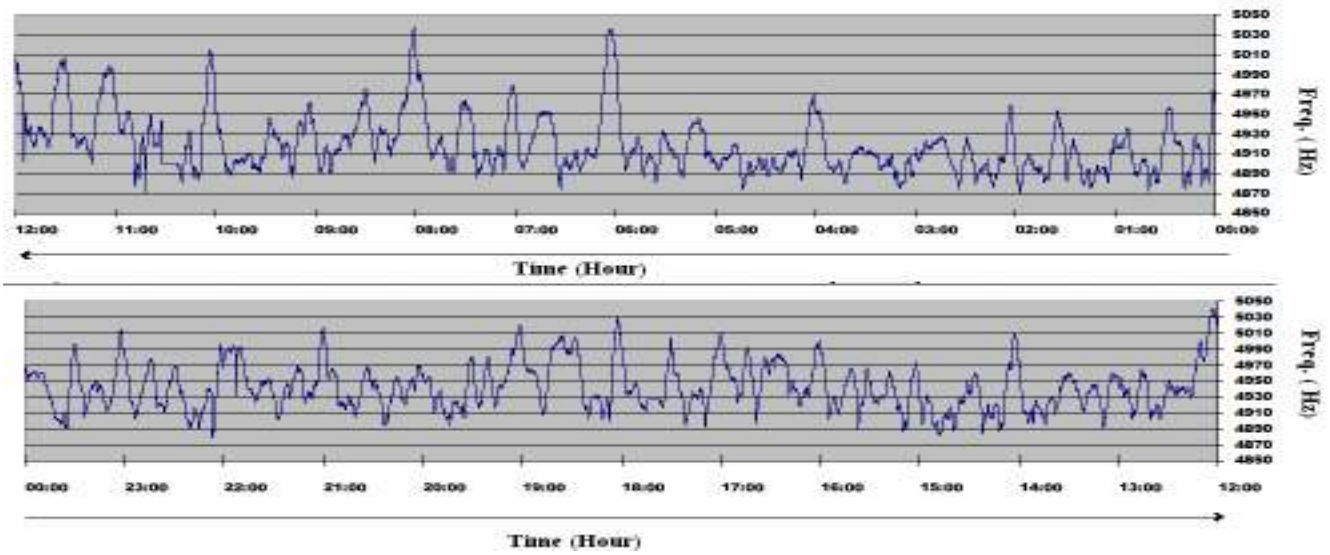

Figure 10:Frequency Chart of 30/6/2008

Conclusion:

The system is reliable and accurate, it is multipurpose instrument. It can be used as a frequency meter, and it is suitable to be operated at line voltage source and an external source (function genirator). The accuracy is higher than the previous type, because the high speed processing of PC. Another very important advantage of using PC is the archiving system which is impoossible in the previous types.

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