STABILITY ANALYSIS OF PARALLEL PWM DC/DC BUCK CONVERTER[+]

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Abstract

This paper presents a new topology for parallel PWM DC/DC buck converter. The topological structure and operation principle of the proposed approach are presented. The stability analysis including Bode plot diagram technique is used to study the performance of this topology.Various design criteria are discussed and verified by computer simulations. It is found that the results are satisfactory, and the proposed topology can be used in high power applications by selecting the applicable values of the controller parameters and number of parallel modules which are needed.

المستخلص

تضمن البحث اقتراحا لتصميم دائرة تحكم لمغير القدرة المتوازية DC/DC الخافض للجهد والمضمن بعرض النبضة مع مبدأ عمل تلك الدائرة. كما تم استخدام تقنية مخطط بود لدراسة استقرارية المنظومة ولقيم مختلفة من معالم التحكم ولعدد المغيرات المربوطة على التوازي. تم مناقشة معايير مختلفة والتحقق منها باستخدام أسلوب المحاكاة الحاسوبية. كانت النتائج مقبولة وان الدائرة المقترحة يمكن استخدامها لمغيرات القدرة العالية عن طريق زيادة عدد المغيرات المربوطة على التوازي.

Introduction

The parallel DC/DC converters have gained increasing attention in the past few years for high power applications [1]. Numerous topologies to realize these converters had been introduced and widely studied [2]. Many advantages are provided in using the parallel DC/DC converter, which can be summarized as follows:

i- Increasing the capability of power processing.
ii- Improved reliability due to more even distribution of stresses.
iii- Enhanced availability from the fault tolerance for the system against the failure of a single converter.

Stability and transient response simulation of the democratic and master slave current sharing had been discussed in [3].

The parallel operation of DC/DC converter using 3-phase rectifier units for telecommunication application was also achieved [4].

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In this paper, a new topology of parallel PWM DC/DC buck converter is studied. The operation and mathematical analysis are performed for the proposed topology. The stability analysis including Bode plot diagram has been presented for different controller parameter values.

The Laplace transform method with numerical method is used to analyze the response of the converter topology.

Small – Signal Model

There are several topologies of DC/DC converter, but PWM DC/DC buck converter is widely used for electronic power supplies [5], since it has simple construction and can be easily controlled.

Fig. (1) presents an open-loop DC/DC buck converter, in which the desired output voltage is small compared to the typical input voltage level. It has a voltage source input and current source output.

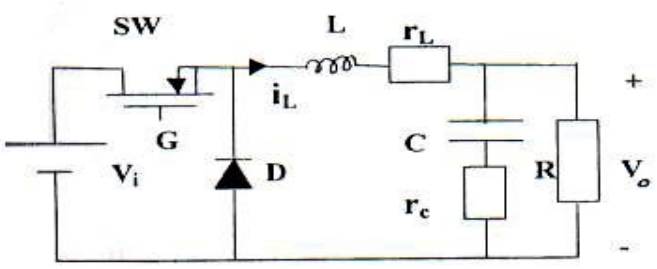

Fig. (1): Single module PWM DC/DC Converter

The transfer function of this small-signal model of PWM DC/DC converter can be derived from the average model of the converter and by assuming that the converter is operated in continuous condition mode only, as follows:

$$L\frac{d i_L(t)}{dt} = D V_i - r_L i_L(t) - v_o(t) \quad \ldots\ldots\ldots\ldots (1)$$

$$C\frac{d v_C(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} \quad \ldots\ldots\ldots\ldots (2)$$

$$r_C C\frac{d v_C(t)}{dt} = v_o(t) - v_C(t) \quad \ldots\ldots\ldots\ldots (3)$$

The state variables of the average converter model can be written as a nominal value plus a small time varying perturbation as follows:

$$v_C(t) = V_C + \Delta v_C(t) \ ;$$
$$v_o(t) = V_o + \Delta v_o(t) \ ;$$
$$i_l(t) = I_L + \Delta i_L(t) \ ;$$
$$v_i(t) = V_i + \Delta v_i(t) \ ;$$
$$i_o(t) = I_o + \Delta i_o(t) \ ; \text{ and}$$
$$d(t) = D + \Delta d(t)$$

So equations (1), (2), and (3) can be rewritten as follows:

$$L\frac{d\Delta i_L}{dt} = D\Delta v_i + dV_i - r_L\Delta i_L(t) - \Delta v_o \text{.....(4)}$$

$$C\frac{d\Delta v_C}{dt} = \Delta i_L(t) - \frac{\Delta v_o}{R} + \Delta i_o \text{.....(5)}$$

$$r_c C\frac{d\Delta v_C}{dt} = \Delta v_o - \Delta v_C \text{.....(6)}$$

Now, the transfer function of open-loop output voltage can be obtained using Laplace transforms:

$$\Delta v_o = H_1(s)\Delta v_i + H_2(s)\Delta d + H_3(s)\Delta i_o \text{.....(7)}$$

where

$$H_1(s) = \frac{c_5(S+c_3)D}{(S^2+c_1S+c_2)} \;;\; H_2(s) = \frac{c_5(S+c_3)V_i}{(S^2+c_1S+c_2)} \;;\; H_3(s) = \frac{-c_6(S+c_3)(S+c_4)}{(S^2+c_1S+c_2)} \;;$$

$c_o = L\,C\,r_c + R\,C\,L$;
$c_1 = (L + r_L\,r_C\,C + R\,C\,r_L + R\,C\,r_C)/c_o$;
$c_2 = (r_L+R)/c_o$;
$c_3 = 1/(C\,r_C)$; $c_4 = r_L / L$;
$c_5 = R\,C\,r_c/c_o$; and
$c_6 = R\,C\,r_c\,L / c_o$

Parallel Topology

The configuration of the paralleling topology is shown in Fig. (2) for two modules PWM buck converter common with the same output capacitor.

Each module contains a buck power stage, PWM modulator inductor current sensor with gain (K_i), and subtractor.

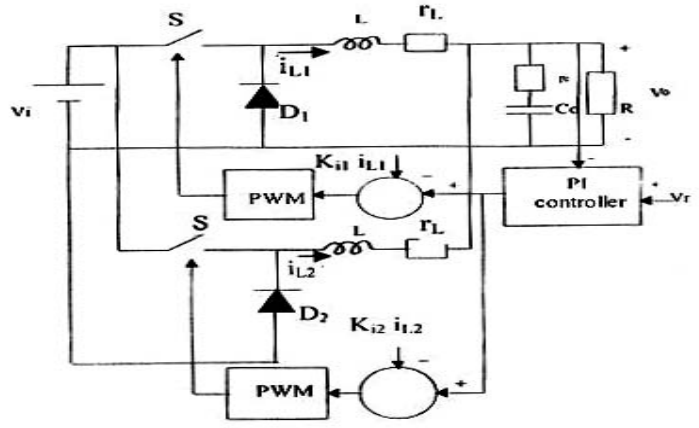

Fig. (2): The proposed system

A common PI controller for all modules is used. The sensed inductor current of each converter is subtracted from the output of the common PI controller. The output of the subtractor feeds a PWM modulator circuit to generate pulses to the desired switching transistor.This parallel topology can be studied using the equations (1) to (7) which are derived above for the small-single model of the converter. Bode plot diagram technique is used to analyze the stability of the topology. The following three criteria for close-loop performance are considered:

i- Open-loop transfer function G(S)H(s).
ii- Dynamic line response $\Delta v_o / \Delta v_i$.
iii- Output impedance $\Delta v_o / \Delta i_o$

In order to analyze the parallel topology, the following assumptions are taken:

$K_{ii} = K_{i1} - K_{i2}$; $U_1 = U_2 = U = 1/n$; and $V_{r1} = V_{r2} = V_r$

The PI controller is presented by $(K_p + K_{in}/s)$. From equation (7), the three criteria of the closed-loop can be derived as follows:

1- The control response (open loop) transfer function of the system is :

$$G(s)H(s) = \frac{c_{13} V_i (s^2 + c_{11} S + c_{12}}{s(s^2 + c_1 S + c_2)} \quad \text{…….. (8)}$$

2- The dynamic line response of the system is:

$$\frac{\Delta v_o}{\Delta v_i} = \frac{c_5 (S + c_3) D}{(s^3 + c_7 s^2 + c_8 S + c_9)} \quad \text{…..… (9)}$$

3- The dynamic load behavior (output impedance) of the system is:

$$\frac{\Delta v_o}{\Delta i_o} = \frac{c_6 S (S + c_3)(S + c_{10})}{(s^3 + c_7 s^2 + c_8 S + c_9)} \quad \text{…… (10)}$$

C = 470 μF , L = 100 μH , V_i = 20 V,
r_c = 0. Where
$c_7 = c_1 + c_5 V_i (K_p + c_{14})$;
$c_8 = c_2 + c_5 V_i (K_{in} + K_p c_3 + c_{14} c_{15} K_i)$;
$c_9 = R V_i K_{in} / c_o$
$c_{10} = c_4 + c_5 V_i K_i / c_6$
$c_{11} = (K_{in} + K_p c_3 + c_{14} c_{15} K_i)$
$c_{12} = K_{in} c_3 / c_{16}$
$c_{13} = c_5 c_{12}$
$c_{14} = 1/R + 1/r_c$
$c_{15} = c_3 / (R c_{14})$
$c_{16} = K_p + c_{14} K_{in}$

The parameter of the power stage of the converter are selected as follows:
C = 470 μF , L = 100 μH , V_i = 20 V,
r_c = 0.04 Ω , r_L = 0.04 Ω , and V_o = 10 V

The stability of the system is detected by determining the cross over frequency and the phase margin. This can be derived from equation (8), as follows:

$w^6 + c_{17} w^4 + c_{18} w^2 = c_{19}$ …… (11)

where

$c_{17} = c_1^2 - 2c_2 - c_{13}^2 Vi^2$;

$c_{18} = c_2^2 + 2c_{13}^2 V_i^2 c_{12} - c_{13}^2 V_i^2 c_{11}$; and

$c_{19} = c_{13}^2 V_i^2 c_{12}^2$

When one solving equation (11) using Newton's method, the cross over frequency of the system is obtained. This value of frequency will be used in equation (8) to determine the phase margin of the system.

Results

The Bode plots diagram for the control transfer function G(s)H(s) and for different values of the controller parameters are shown in Fig. (3). It is shown that the variation in the controller parameters and in the number of module (n) will keep system in the stable region and only the cross over frequency is changed.

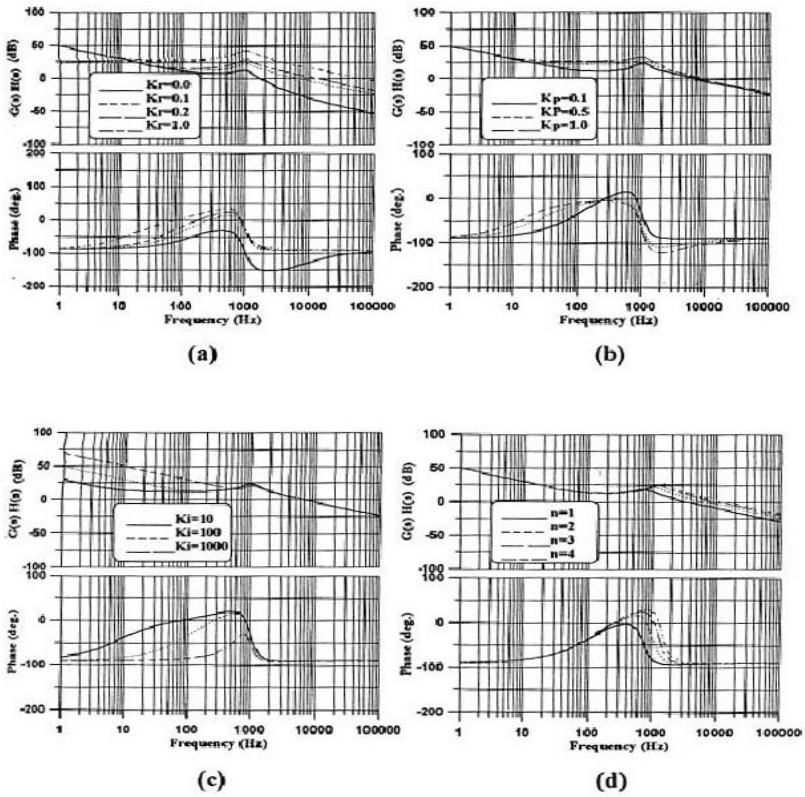

Fig. (3): Bode plots of control response when R = 1 Ω

(a) Different values of K_i, n=2, K_p=0.1,and K_{in}=100 **(b)** Different values of K_p, n=2, K_i=0.1, and K_{in}=100
(c) Different values of K_{in}, n=2, K_p=0.1,and K_i=0.1 **(d)** Differen values of n, K_p=0.1, K_i=0.1,and K_{in}=100

The dynamic line response and the dynamic load behavior of the system for different number of paralleling converters are shown in Fig. (4). This figure shows that the perturbation introduced in the input supply voltage or load disturbance has approximately the same effect on the system for different number of modules.

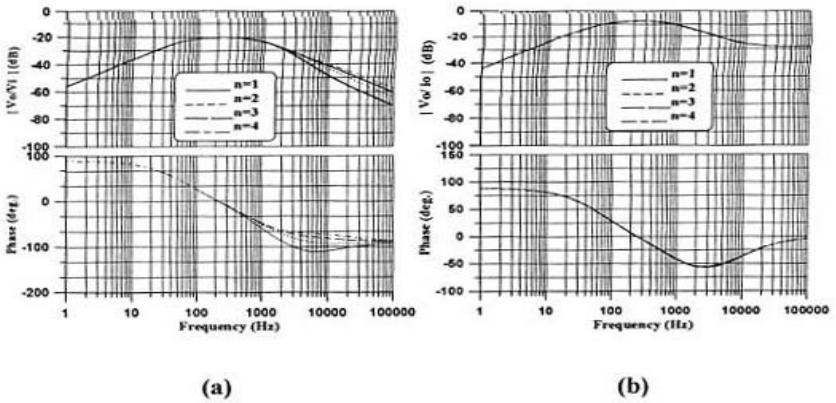

Fig. (4): Bode plots when R=1Ω, K_p= 0.1, K_i=0.1, and K_{in}=100

(a) Dynamic line response **(b)** Dynamic load behavior

The inductor current of the two paralleling converters is shown in Fig. (5). This figure shows that the system is stable when K_{in} = 100.

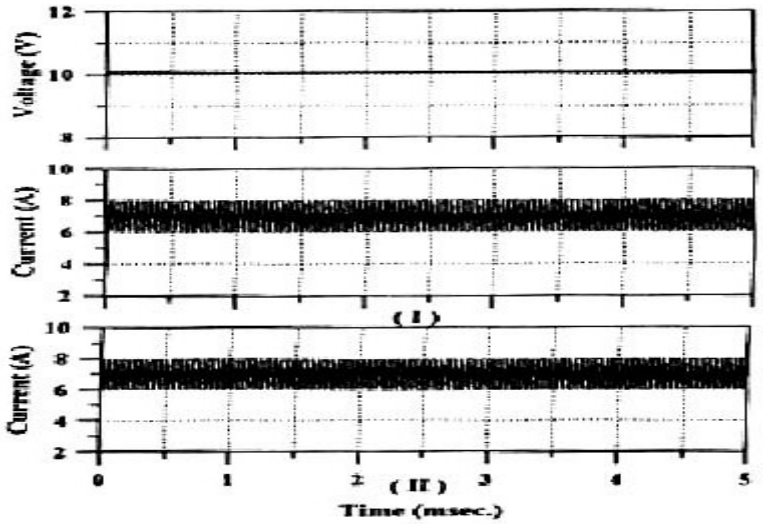

Fig. (5): Inductor current and output voltage when n=2, R = 1 Ω,

K_p = 0.1, K_{i1}=K_{i2}=0.1,Kin=100, and V_r=10 V (I) Converter 1. (II) Converter 2

Conclusion

In this paper, a new topology of parallel PWM DC/DC buck converter is presented. The stability analysis including Bode plot diagram has been discussed using a small-signal model. The computer simulation results indicate that the parallel topology is stable for wide range of controller parameters, and the increase in the number of parallel modules has a small effect on the stability. It is clear that the system has satisfactory results and can be used in high power applications.

List Of Symbols

C Smoothing capacitor, F.
D Duty cycle.
D_1,D_2 Converter diodes.
Δd Perturbed duty cycle value.
Δi_L Perturbed inductor current value, A.
Δi_o Perturbed output current value, A.
Δv_i Perturbed input voltage value, V.
Δv_o Perturbed output voltage value, V.
Δv_r Perturbed reference voltage value, V.
F_s Switching frequency, Hz.
i_L Inductor current, A.
I_r Reference value for the direct clipping current, A.
V_o Output voltage, V.
I_c Common reference current, A.
K_{in} Integral controller gain.
K_p Proportional controller gain.
K_i Current controller gain.
L Converter inductor, H.
R Load resistance, Ω.
r_c ESR of the smoothing capacitor, Ω.
r_L Converter inductor series resistance, Ω.
t Instantaneous time, sec.
T_s Total switching period time, sec.
v_c Feed-forward signal, V.
V_i Input voltage, V.
V_r Input reference voltage, V.

References

1- V. J. Thottuvelil and G. C. Verghese, " Analysis and Control Design of Parallel DC/DC Converters with Current Sharing", *IEEE Trans. on Power Electronics*, Vol.13, pp. 635-644 , July, 1998 .
2- B. Choi, " Comparative Study on Parallel Schemes of Converter Modules for Distributed Power Applications", *IEEE Trans. on Power Electronics*, Vol-45, No. 2, pp. 194-199 , April, 1998.
3- A. J. Nascimento Jr, and V. J. Farias, " PWM Control for Parallel Converter in the Current Sharing Mode", *COBEP, 5 th Brazilian Power Electronics Conference* , 1999.
4- M. L. Heldwein, A. F. DE Souza, and I. Barbi , " A Simple Control Strategy Applied to Three Phase Rectifier Units For Telecommunication Application Using Single-Phase Rectifier Modules", *IEEE PESC* , pp. 795-800 , 1999.
5- Y. T. Chen, and F. Y. Shih, "New Multi-Output Switching Converters with MOSFET-Rectifier", *IEEE Trans. on Ind. Elec*., Vol. 45 , No. 4, pp. 609-616 , Aug,1998.