IMPLEMENTATION OF A SOFT - SWITCHING FOR PW INVERTER[+]

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Abstract

The purpose of this paper is to suggest, develop, implement a novel soft-switching PWM inverter suitable for practical applications such as control of switched reluctance motor. The suggested circuits of soft switching and the points that must be taken in to account during soft switching implementation quoted in this paper give minimum losses during switch on/off of the power device. Comparison is made between hard switching and soft switching inverter topologies. The novel topology is presented and the principle of operation is described. P-Spice program is used to investigate the circuit.

المستخلص

الهدف من هذا البحث تطوير وتنفيذ طريقة الاشتغال الناعم في العواكس التي تعمل بتضمين عرض النبضة والملائمة للتطبيقات العملية كالسيطرة على سرعة المحركات ذات المعاوقة المغناطيسية. الدائرة المقترحة التي تنفذ عملية الاشتغال الناعم تمت دراستها وكذلك النقاط الواجب اتخاذها لتقليل الخسائر أثناء عملية الاشتغال اجريت مقارنة بين عمليتي الاشتغال بشكل حاد وبشكل ناعم لمعرفة الفرق بين العمليتين باستخدام برنامج (P-Spice) لتمثيل الدائرة وفحصها لمعرفة النتائج.

Introduction

It is desirable for power converters to have high efficiencies and high power densities. Packaging and cost limitation require that the converter have a small physical size and weight. Power density and electrical performance are dependent on the switching frequency as it determines the values of the reactive components in the converter. Thus high frequency operation of the converter is highly desired. However, operation at high frequency results in higher switching losses and higher switching stresses by the circuit parasites (stay induction, junction capacitance).

The main factors that contribute to the high – frequency switching losses are:

- Semiconductor devices that have non-zero turn on and turn off times and thus there is a finite time during the transitions where in the devices are conducting a significant current while a large voltage is applied across it. This results in large energy dissipation. This energy loss increases with increasing frequency.
- At high frequencies, high dv/dt and di/dt induce voltage and current oscillations, in parasitic capacitors and inductors during switching transitions. These oscillations result in

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higher peak current and voltage in the devices and thus the switching loss increases. Furthermore, these oscillations create EMI (Electro magnetic interference) noise, which can interfere with other parts of the circuit and surrounding electronic and equipment.

- When a device is turned on while having a voltage across it, the energy stored in the parasitic capacitance across the switch is dissipated in it. This loss increases with the frequency and is proportional to the square of the voltage across the device before turn-on. [1,2,3,4]

Soft switching techniques

Soft switching forces the switch voltage or current to zero before the device switching, thus avoiding current and voltage overlap during the switching transition. The advantages of soft switching are as follows: -

- Lower switching losses due to smaller overlap of switch voltage and current.
- Lower dv/dt and di/dt and thus lower voltage spike and EMI emissions.
- High reliability due to reduced stresses on the switching components.
- Reduced voltage and current ratings for the devices.
- Smaller reactive elements.

Soft switching for the power devices can be achieved by either zero-voltage switching (ZVS) or zero-current switching (ZCS). ZVS consists of turning on the switches while the voltage across them is zero. ZCS consists of turning off the switches when the current through them is zero. Common to all approaches of soft switching is the use of reactive elements to shape the current and voltage waveforms to achieve the necessary condition for ZVS or ZCS.

Soft switching has been proven to be an effective means of reducing switching losses and of attaining higher overall efficiencies. Various soft switching techniques have been developed in the recent years [1,5].

Principle of operation

Figure (1) shows the proposed soft-switching topology. This is an inverter for a 3-phase operation. The resonant leg is just an add-on to the classic inverter. There are two switches per phase, in addition to two freewheeling diodes for the de-fluxing operation. The resonant branch is connected across the three phase windings to be controlled. A zero voltage turn-on (ZVT) condition is achieved for the main switches by current injection from the auxiliary switch. Thus, this topology achieves (ZVT) for the main switches. IT also achieves zero current turn-off for the auxiliary device [6,7,8].

Capacitors are placed across all main switches and diodes. These form a part of the resonant circuit and are necessary to achieve the ZVT (zero voltage transion) condition for the main switches. Furthermore, they act as lossless snubber capacitors during turn-off. The main feature of this topology is that we can achieve near zero voltage turn-on for the main switches under different load conditions, without utilizing variable timing control. Thus, control for this topology is relatively simple when compared to other soft-switching topologies, which require variable timing control for their operation.

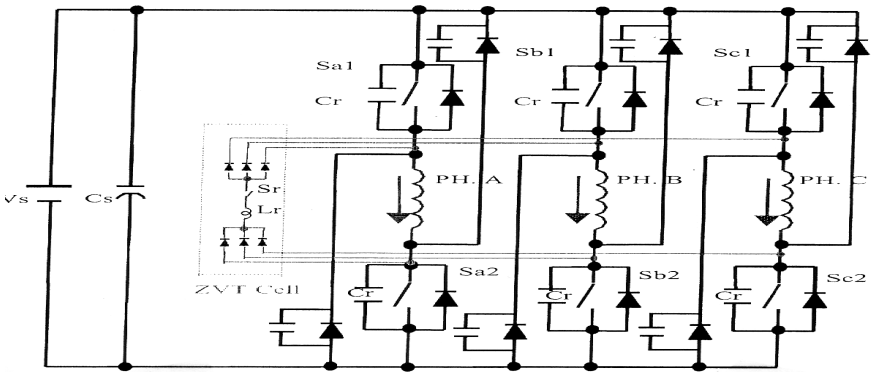

Fig. (1): Proposed soft-switching topology

Figure (2) shows one phase of the proposed inverter, along with the soft – switching leg. It consists of two main switches S_1, S_2 and two freewheeling diodes D_1 and D_2. S_1 and S_2 are switched on and off together.

The basic operation of this circuit consists of turning on the auxiliary switch a fixed time ahead of the main switches. The auxiliary resonant circuit brings the voltage across the main switches to zero, enabling them to be turned on at zero voltage. During turn-off the capacitors across the main switches act as lossless snubbers and this reduces the turn-off losses. Thus, this inverter achieves near zero voltage turn-on and reduces the turn-off losses, thereby appreciably reducing the switching losses in the inverter.

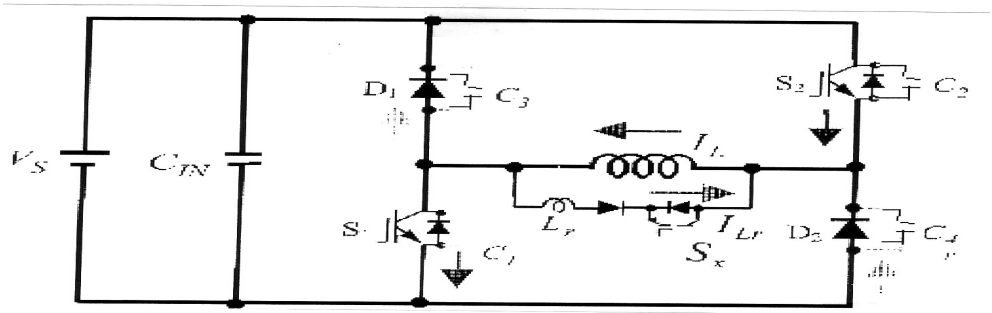

Fig. (2): single phase of the proposed soft switching inverter

Figure (3) shows the important waveforms of this circuit during one cycle. It is assumed that the load current stays constant during this switching cycle.

The different modes of operation can be explained as follows:

Mode 1: t_0-t

Here, the main switches, S_1 and S_2, are in the off state and the load current is being freewheeled through the diodes D_1 and D_2.

Mode 2: t_1-t_2

The auxiliary switch is turned on and current starts to build up linearly in the auxiliary branch. The current in the diodes D_1 and D_2 is falls linearly. The load current is slowly diverted from the freewheeling diodes to the auxiliary branch.

Mode 3: t_2-t_3

At t_2, the inductor (auxiliary) current equals the load current through the diodes. It becomes zero. Thus the diodes turns-off under zero current condition. The resonant inductor, Lr, resonates with the capacitors across the switches and diodes. During this process, the capacitors discharge and thus the voltage across the capacitors decreases.

Mode 4: t_3-t_4

At t_3, the capacitors discharge fully and thus the voltage across the switches becomes zero. The switches can now be turned on under zero voltage condition. As it is difficult to turn on the switches at this particular instant, only near zero voltage switching can be achieved. After the switches are turned on the resonant inductor current I_{Lr}, decreases linearly. At t_4, this current becomes zero and the switches carry the load current I_L.

Mode 5: t_4-t_5

The resonant current I_{Lr} dies down to zero at t_4. After a finite time the auxiliary switch is turned off. Thus the auxiliary switch is turned off at zero current condition. Furthermore, the auxiliary diode is also turned off at zero current condition.

Mode 6: t_5-t_6

Here, the main switches conduct the load current and the circuit is in steady state.

Mode 7: t_6-t_7

The main switches are turned off under hard switching. The lossless snubbers absorb the load current until the diodes $D_1$and D_2 are turned on, the operation then returns to mode 1.

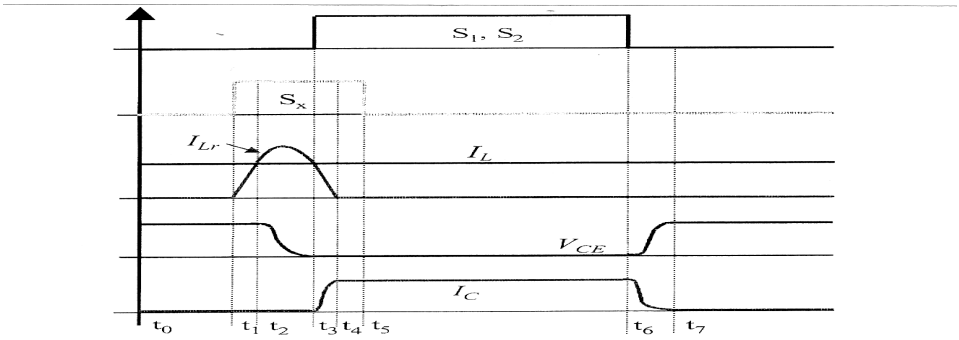

Fig. (3): Wavefrom of the proposed topology

Design of the resonant circuit

The resonant components in this circuit are the resonant inductor Lr, and the resonant capacitor Cr. These values have to be designed to get a highly efficient switching. Wr (resonance frequency) and Zr (resonance impedance) are defined as follows:

$$W_r = \frac{1}{\sqrt{Lr.Cr}} \qquad \ldots\ldots\ldots\ldots \quad (1)$$

$$Z_r = \sqrt{Lr / Cr} \qquad \ldots\ldots\ldots\ldots \quad (2)$$

From equation (1,2), we know that the maximum resonant current would be:

$$I_{Lrmax} = I_L + \frac{Vs}{Zr} \qquad \ldots\ldots\ldots \quad (3)$$

We can rate our resonant switch with this information. As the resonant auxiliary switch carries this peak current only during switch transition, it can be rated for much lower continuous current rating. The timing sequence of the auxiliary switch is determined by calculating the time during each made of operation. The auxiliary switch is turned on at t_1 and the resonant current, I_{Lr}, starts building up linearly until time t_2. At t_2, I_{Lr} equals the load current. Thus the time period T_1 required for the resonant current to reach the load current is calculated by:

$$T_1 = (t_2 - t_1) = \frac{Lr \times I_L}{Vs} \qquad \ldots\ldots\ldots \quad (4)$$

Next the resonant time has to be calculated. This depends on the value of the resonant components. The resonant time period, T_2 is given by the equation:

$$T_2 = (t_3 - t_2) = \pi \times \sqrt{Lr \times Cr} \qquad \ldots\ldots\ldots \quad (5)$$

The time required for the resonant current to die down to zero, T_3, would be equal to T_1 and can be calculated by:

$$T_3 = (t_4 - t_3) = \frac{Lr \times I_L}{Vs} \qquad \ldots\ldots\ldots \quad (6)$$

Now the auxiliary switch is turned off at a finite time after t_4. Thus the total calculating time period of the auxiliary switch T would be calculated by:

$$T = T_1 + T_2 + T_3 \qquad \ldots\ldots\ldots \quad (7)$$

Thus, T is a function of the load current and the value of the resonant components. For getting the exact time sequence, the resonant inductor and capacitor values have to be selected. The first component to be designed is the resonant capacitor.This capacitor forms a part of the resonant circuit during turn-on and also acts as lossless snubber during turn-off. During turn-off the value of the capacitance is inversely proportional to the rate of rise of the switch voltage. This in turn reduces the turn-off losses. Hence we need to be capacitance increase, there is more energy stored in it.

This energy would be discharged during turn on and thus adds to the turn on losses. Thus an optimum value of the capacitance has to be chosen which would reduce the turn-off losses, while not affecting the turn-on adversely.

The D.C supply of 165v will be chosen and the switches are to be designed for 8A continuous current. By trying different values of capacitance and by judging the performance, a value of 22 nF is chosen. This value is big enough to reduce the turn-off losses significantly and is small enough not to be adversely affect the turn-on. After selecting this value, the selection of the resonant inductor depends upon the allowable peak current through it.

Allowing for a peak current of 20A, we get a value of 13.75 for Zr. Given the value of resonant capacitance 22nF, this translates to a resonant inductance of 4.16μH. With these

values, the resonant time T_2 is 0.95us. Thus, the different time periods during the resonant cycle are as follows:

$T_1 = 0.2\mu s$
$T_2 = 0.95\mu s$
$T_3 = 0.2\mu s$

Thus T has to be greater than 1.35μs. All the resonant components have thus been designed.

Results

The proposed topology is verified by simulating the single-phase operation in P – Spice. Simulation is done using the real physical components with hard and soft switching techniques. Figure (4) shows the voltage across the switch and the current through the switch during hard switching period. It shows the voltage and current overlap during the switching interval.

The extents of this overlap determine the switching losses during this transition. Figure (5) shows the corresponding waveforms during turn-off. As the switching frequency increases, the switching losses become a major part of the overall losses and thus the efficiency of the system decreases considerably. The proposed topology would considerably decrease these switching losses by reducing the voltage current overlap during this switching.

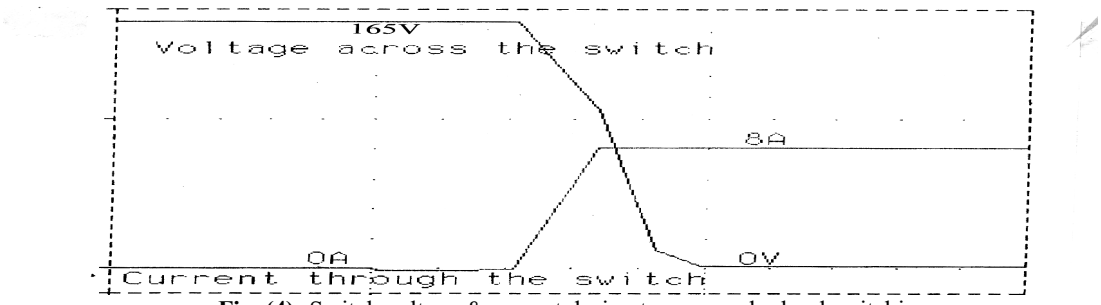

Fig. (4): Switch voltage & current during turn on under hard switching

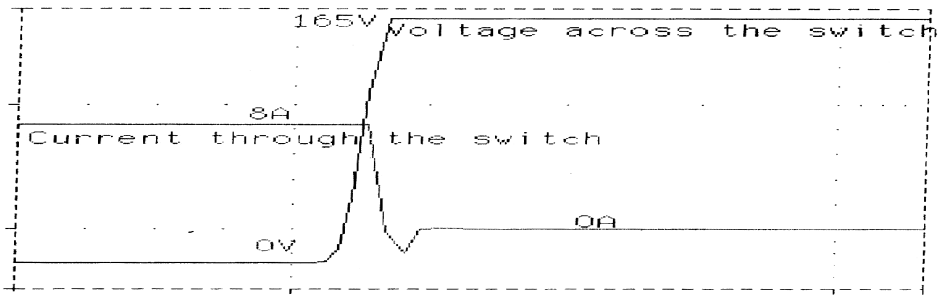

Fig. (5): Switch voltage & current during turn off under hard switching

The soft switching technique is used on auxiliary resonant branch to create a zero voltage turn-on for the main switches. Figure (6) shows the gate voltages of the main and auxiliary switch.

The time difference between these two signals is calculated in the last section and it is equal to T_1+T_2. For the given case, the value was found to be 1.15μs. The auxiliary pulse has to be greater than 1.35μμs and it has been fixed at 2μs in this case. Figure (7) shows the main switch gate voltage and the main switch drain to-
source voltage during turn-on.

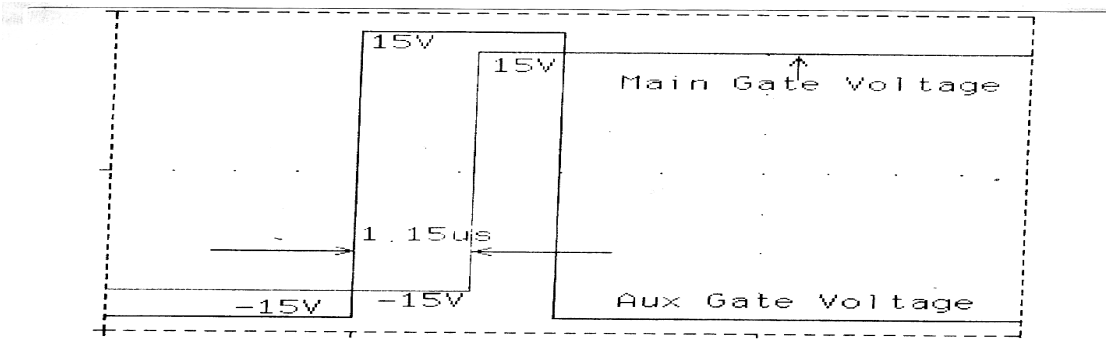

Fig. (6): Gate voltage for the main & auxiliary switches

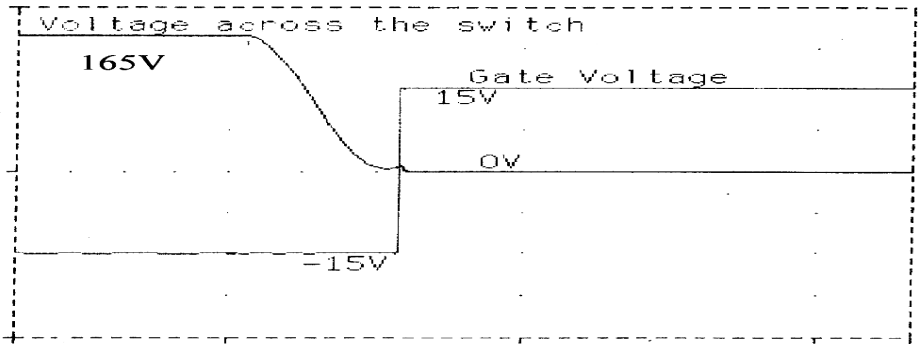

Fig. (7): Gate & switch voltage during turn on under soft switching

In this case, the voltage across the switching begins to decrease and is very close to zero before the gate voltage is applied. Thus the switch is turned on at near zero voltage condition. Figure (8) shows the voltage across the switch and the current through it for the same switching period. Here, the voltage current overlap is very small and thus the switching loss is less, compared to the hard switching case. Figure (9) shows the waveforms during turn-off. The voltage – current overlap here is considerably smaller than in the hard switching case. Thus, the turn-off switching loss is much lower with soft switching. The timing sequence in this soft-switching circuit is very important. If it is not adjusted properly, the switching losses would not be minimized.

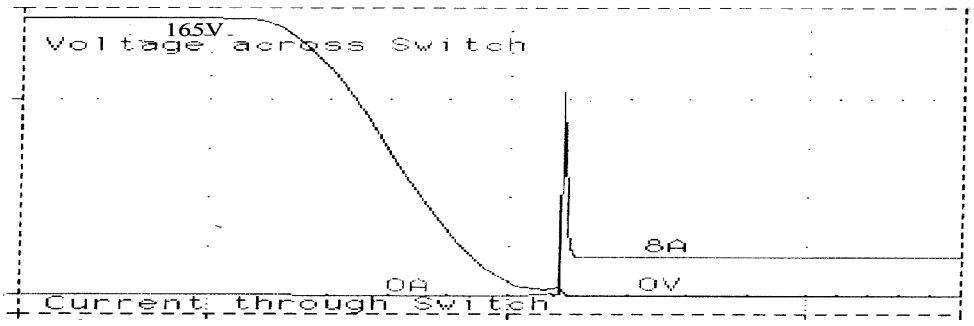

Fig. (8): Switch voltage & current during turn on under soft switching

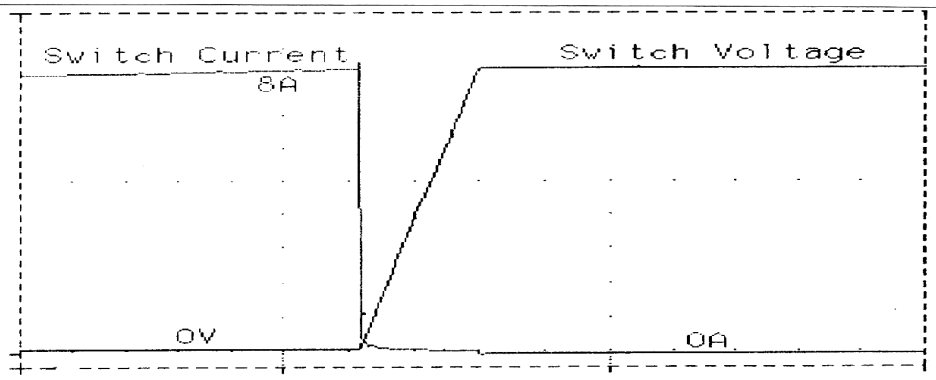

Fig. (9): Switch voltage & current during turn off under soft switching

Conclusion

A novel soft-switching topology is presented and its principle of operation is explained. The designed soft-switching circuit is verified using P–Spice program. The comparison between the hard switching and soft switching Techniques is investigated. The turn-on and turn-off losses is significantly minimized because of very small voltage current overlap period, Hence the efficiency of the inverte has improved especially in high frequency operation. The timing sequence in this soft-switching circuit is very important. If it is not adjusted properly, the switching losses would not be minimized.The following observations are made:

- A near zero voltage turn-on is achieved for the main switches.
- Turn-off losses are reduced by using the snubber capacitor.
- Freewheeling diodes turn off under zero current condition and this greatly reduces the reverse recovery problem of the diodes.
- Auxiliary switch turns off under zero current condition.
- Auxiliary diodes turn-off under zero current condition.
- Due to all the above effects, the switching losses are considerably reduced.
- Soft switching results in considerably less noise than hard switching case.

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